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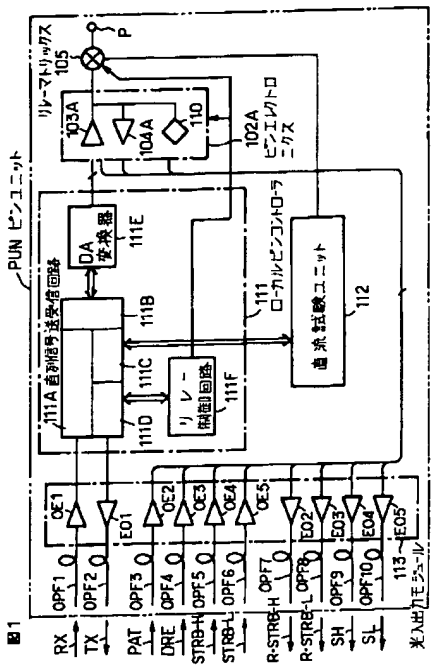
(54)【発明の名称】　集積回路デバイス試験装置

(57)【要約】
【課題】　メインフレームとテストヘッドの間を接続するケーブル群を細く、且つ長距離に延長することができる集積回路デバイス試験装置を提供する。
【解決手段】　メインフレーム２００とテストヘッド１００との間で授受する信号の全てを光信号に置換し、光ファイバケーブルによって信号伝送路を構成してテストヘッドに接触させた被試験集積回路デバイスを試験する構成とした。



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【特許請求の範囲】

【請求項１】　パターン発生器を格納したメインフレームと、このメインフレームから離れて設置され、被試験デバイスを接触させて、その試験を行うテストヘッドとを具備して構成される集積回路デバイス試験装置において、

上記メインフレームとテストヘッドとの間の信号伝送路の全て、または一部を光信号路によって構成したことを特徴とする集積回路デバイス試験装置。

【請求項２】　請求項１記載の集積回路デバイス試験装置において、上記メインフレームからテストヘッドに送り込む各端子ごとに設定するデータを光の直列信号で伝送し、テストヘッド側に設けた直列送受信回路で受信し、並列信号に変換してレジスタ群にストアするように構成したことを特徴とする集積回路デバイス試験装置。

【請求項３】　請求項１または２記載の集積回路デバイス試験装置の何れかにおいて、テストヘッド側に直流試験ユニットを設け、この直流試験ユニットへの制御信号をメインフレーム側から光の直列信号で伝送し、直流試験ユニットを制御して被試験デバイスの直流試験を実行する構成としたことを特徴とする集積回路デバイス試験装置。

【請求項４】　請求項３記載の集積回路デバイス試験装置において、各端子ごとに設定するデータ及び直流試験結果をテストヘッド側のレジスタ群にストアすると共に、その設定データ及び直流試験結果を上記直列送受信回路でメインフレームに光の直列信号として伝送するように構成したことを特徴とする集積回路デバイス試験装置。

【請求項５】　請求項４記載の集積回路デバイス試験装置において、被試験デバイスに与えるパターン信号を各端子毎に光の直列信号としてメインフレームからテストヘッドに供給し、テストヘッドに設けたドライバを通じて被試験デバイスに与えると共に、被試験デバイスから読み出した読み出し信号をテストヘッドに設けたアナログ比較器で正規のＨ論理電圧及びＬ論理電圧を持っているか否かを判定し、その判定結果を各端子毎に電気－光変換器で光の直列信号に変換し、光伝送路を通じてメインフレームに伝送する構成としたことを特徴とする集積回路デバイス試験装置。

【請求項６】　請求項３記載の集積回路試験装置において、テストヘッドに被試験デバイスの各端子に対応して第２直列信号送受信回路と波形整形回路及び論理比較器とを設け、メインフレームからディジタルのパターンデータを各端子ごとにテストヘッドに光の直列信号で伝送し、テストヘッドにおいて上記第２直列信号送受信回路で受信して並列パターンデータに変換し、この並列パターンデータを上記波形整形回路でアナログのパターン信号に変換し、このパターン信号をドライバを通じて被試験デバイスの各端子に与えると共に、被試験デバイスの

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読み出し信号をアナログ比較器で論理レベルが正常か否かを判定し、その判定結果を論理比較器でメインフレームから送られて来るディジタルの期待値パターンデータと論理比較し、その論理比較結果を上記第２直列信号送受信回路を通じて光の直列信号としてメインフレームに伝送する構成としたことを特徴とする集積回路デバイス試験装置。

【請求項７】　請求項６記載の集積回路デバイス試験装置において、テストヘッドにタイミング発生器を設け、このタイミング発生器にメインフレームから光の直列信号で伝送したディジタルのタイミングデータを上記第２直列信号送受信回路で並列信号に変換して与え、タイミング発生器から出力されるタイミング信号に従って上記波形整形回路、論理比較回路、アナログ比較回路の動作を制御する構成としたことを特徴とする集積回路デバイス試験装置。

【請求項８】　請求項７記載の集積回路デバイス試験装置において、テストヘッドにパターンメモリ、フェイルメモリ、タイミングメモリを設け、パターンメモリ及びタイミングメモリにメインフレームから予めパターンデータ及びタイミングデータを光信号で伝送して記憶させ、試験の開始と共に、これらのメモリからパターンデータとタイミングデータを読み出し、波形整形回路及びタイミング発生器においてパターン信号とタイミング信号を生成し、被試験デバイスの機能試験を実行すると共に、機能試験の結果を論理比較回路から得、この試験結果を上記フェイルメモリに記憶させ、その記憶を光信号でメインフレームに伝送することを特徴とする集積回路デバイス試験装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】この発明は半導体集積回路デバイス（ＩＣ）乃至は大規模集積回路デバイス（ＬＳＩ）を試験する集積回路デバイス試験装置に関する。

【０００２】

【従来の技術】図７に一般的な集積回路デバイス試験装置の概略の構成を示す。図中１００はテストヘッド、２００はメインフレームと呼ばれる部分をそれぞれ示す。テストヘッド１００にはパフォーマンスボード１０１とピン・エレクトロニクス１０２が搭載される。パフォーマンスボード１０１には被試験デバイスＤＵＴを接触させるソケットが装着され、このソケット（図には特に示していない）を通じて被試験デバイスＤＵＴと試験装置とが電気的に接続される。

【０００３】ピン・エレクトロニクス１０２には一般に被試験デバイスＤＵＴを電気的に駆動するドライバ群１０３と、被試験デバイスＤＵＴから読み出される応答出力信号のＨ論理及びＬ論理が正規の電圧値を持っているか否かを判定するアナログ比較器群１０４と、被試験デバイスＤＵＴの各端子に接続する装置群を切替えるリレ

ーマトリックス１０５とが格納される。

【０００４】メインフレーム２００にはパターン発生器２０１が設けられ、このパターン発生器２０１からテストパターンデータ（ディジタル信号）が出力される。このテストパターンデータと、タイミングエッジ信号は波形整形回路２０２に入力され、この波形整形回路２０２で被試験デバイスＤＵＴの各端子に与えるパターン信号（アナログ波形を持つ信号）を生成させる。このパターン信号がパターン伝送路３０１を通じてテストヘッド１００に送り出され、ドライバ群１０３を通じて被試験デバイスＤＵＴの各端子に与えられる。尚、このパターン伝送路３０１には同時にタイミング信号も伝送される。

【０００５】アナログ比較器群１０４の比較結果は応答信号伝送路３０２を通じてメインフレーム２００に返送され、論理比較回路２０３でパターン発生器２０１が発生する期待値パターンと論理比較し、不一致の発生を検出して不良個所を検出する。２０４はフェイルメモリを示し、論理比較回路２０３で不一致が発生するごとにその不良が発生したアドレスに不良を表す例えばＨ論理を書き込む。

【０００６】２０５はタイミング発生器を示す。このタイミング発生器２０５に関しては、後にこの発明で粗遅延回路ＤＹ１と微遅延回路ＤＹ２をメインフレーム２００とテストヘッド１００とに分離して設置することを説明する都合上、粗遅延回路ＤＹ１と微遅延回路ＤＹ２の存在を予め説明する。従来よりタイミング発生器２０５では、図８Ａに示す基準クロックＣＬＫを分周してテスト周期Ｔを決定するレートパルスＲＡＴ（図８Ｂ）を得ると共に、このレートパルスＲＡＴを任意の時間遅延させて各種のタイミング信号、例えばテストパターン信号の波形の立上りのタイミング、立下りのタイミング、アナログ比較器群１０４のストローブのタイミング、論理比較回路２０３の比較動作のタイミング等を発生させる。

【０００７】従って、タイミング発生器２０５にはレートパルスＲＡＴをテスト周期ＴＫの範囲内あるいは、数倍の範囲で任意の時間遅延させることができる遅延回路が多数設けられ、これら多数の遅延回路によって基準タイミングから任意の時間遅延した例えば図８Ｃ，Ｄに示すような各種のタイミング信号Ｔ１，Ｔ２を生成させている。

【０００８】タイミング発生器２０５に設けられる多数の遅延回路はクロックＣＬＫを計数して、クロックＣＬＫの周期τ_1を単位とする遅延時間を与える粗遅延回路ＤＹ１と、クロックＣＬＫの周期τ_1の範囲内を更に細かく分割して遅延時間を規定する微遅延回路ＤＹ２の組み合わせによって構成され、例えばピコ秒単位の分解能でテストパターン信号の立上り、立下りのタイミング等を規定している。

【０００９】メインフレーム２００にはその他に直流試験ユニット２０６と、負荷試験ユニット２０７，パターン信号のＨ論理とＬ論理の電圧値ＶＩＨ，ＶＩＬを設定する第１基準電圧源２０８と、アナログ比較器群１０４に比較電圧ＶＯＨ，ＶＯＬを与える第２基準電圧源２０９と、被試験デバイスＤＵＴを動作させるための電圧を与える電源装置２１１とが設けられる。

【００１０】

【発明が解決しようとする課題】図９にテストヘッド１００とメインフレーム２００の接続状況を示す。メインフレーム２００とテストヘッド１００との間はケーブル群３００で接続される。図７で説明したようにメインフレーム２００とテストヘッド１００との間には各種の信号線が存在するため、ケーブル群３００に収納されるケーブルの本数は多くなる。

【００１１】また、半導体集積回路デバイスの集積度の向上と共に、デバイスの端子数が増加する傾向にある。更に動作速度の向上もあるためメインフレーム２００とテストヘッド１００との間を接続するケーブル群３００のケーブルの本数も増加の傾向にある。例えば１０００端子分のテスト容量を持つ試験装置では、メインフレーム２００とテストヘッド１００との間で授受される信号の数は数万の数に及ぶ、しかもそれぞれに高速性、高精度、耐ノイズ性等を考慮してツイストペア、同軸ケーブル、多重シールド等の特殊ケーブルが用いられるから、実質的な導体数は信号数の数倍になり、ケーブル群３００は巨大な束となり、テストヘッド１００の移動（ハンドラの取付け、取外し等）を困難なものとしている。

【００１２】また、ケーブル群３００を少しでも長くするとケーブル間のクロストークも増加し、試験精度を劣化させる不都合もある。更に、これらの大量の信号を伝送するには大電力を必要とし、これは発熱量の増加を意味し、冷却を困難としており、また終端抵抗器の数も多くなるため、システムの小型化を阻害する要因となっている。

【００１３】この発明の目的は、メインフレームとテストヘッドとの間を接続するケーブル群を極小化し、テストヘッドの取扱いを容易にすると共に、信号間のクロストークの発生も抑えることができる集積回路デバイス試験装置を提供しようとするものである。

【００１４】

【課題を解決するための手段】この発明ではメインフレームとテストヘッドとの間の信号伝送路の全て、或いは一部を高速伝送に適した光信号伝送路に置き換え、光信号によってメインフレームとテストヘッドとの間の信号の授受を行わせるように構成するものである。この発明ではメインフレームからテストヘッドに送り込む各端子ごとに設定するデータ或いは各種タイミング信号を光の直列信号で伝送し、テストヘッド側に設けた直列受信手段で受信し、並列信号に変換して設定レジスタにストアすると共に、測定データ、測定結果を光信号で返送する

構成とした集積回路デバイス試験装置を提供するものである。

【００１５】この発明では更にテストヘッド側にパターンメモリと波形整形回路とを設け、パターン発生器が出力するディジタルのテストパターンデータを光の直列信号でテストヘッドに伝送し、パターンメモリに記憶させる。試験開始と共に、このパターンメモリに記憶したテストパターンデータを読み出し、その読み出したテストパターンデータ（ディジタル信号）と波形整形回路でアナログのパターン信号に変換し、このパターン信号をドライバ群を通じて被試験デバイスＤＵＴに印加するように構成した集積回路デバイス試験装置を提供する。

【００１６】この発明の構成によれば光信号伝送路はプラスチック光ファイバを用いたとしても、その直径は２００～５００μｍφ程度であり、また電気信号のように、各チャンネルごとに往復導体を必要としないから、信号伝送路の形態は小径化及び軽量化することができる。特に光の直列信号で授受する構成とすることにより、光ファイバの本数を少なくできるから、更にケーブル群の径を小さくでき、軽量化も達することができる。また、光ファイバは中心部分のみを光が伝達するため相互にクロストークの発生がない。従って、延長距離を長くできる利点も得られる。

【００１７】

【発明の実施の形態】図１にこの発明の一実施例を示す。図はテストヘッド１００側の１つの端子（被試験デバイスＤＵＴの１つの端子Ｐ）にパターン信号を供給し、また、この端子から出力された信号をアナログ比較してメインフレーム２００に送る部分（以下この部分をピンユニットＰＵＮと称す）の構成を示す。

【００１８】ピンユニットＰＵＮにはこの例では、被試験集積回路デバイスＤＵＴの１つの端子Ｐを駆動するドライバ１０３Ａ及びアナログ比較器１０４Ａ，負荷試験回路１１０とを搭載したピンエレクトロニクス１０２Ａと、リレーマトリックス１０５に加えて、ローカルピンコントローラ１１１と、直流試験ユニット１１２と、光入出力モジュール１１３とを設けた場合を示す。

【００１９】光入出力モジュール１１３は光・電気変換器ＯＥ１～ＯＥ５と、電気・光変換器ＥＯ１～ＥＯ５とを有し、メインフレーム２００から送られて来る光信号を光・電圧変換器ＯＥ１～ＯＥ５にて電気信号に変換し、その電気信号を利用して機能試験と直流試験を実行させる。ローカルピンコントローラ１１１は光ファイバＯＰＦ１から光・電圧変換器ＯＥ１を通じて送られて来る直列信号を受け取る直列信号送受信回路１１１Ａと、この直列信号送受信回路１１１Ａで受け取った各種の設定データを取り込むレジスタ群１１１Ｂ，１１１Ｃ，１１１Ｄと、レジスタ群１１１Ｂに取り込んだ設定データにより、例えばドライバ１０３Ａに与える電圧ＶＩＨ，ＶＩＬ及びアナログ比較器１０４Ａに与える比較電圧ＶＯＨ，ＶＯＬ等を発生するＤＡ変換器１１１Ｅと、レジスタ群１１１Ｄに取り込んだリレー制御信号によりリレーマトリックス１０５の状態を制御するリレー制御回路１１１Ｆとを具備して構成することができる。

【００２０】つまり、レジスタ群１１１Ｂにはドライバ１０３Ａに与えるＨ論理の電圧ＶＩＨとＬ論理の電圧ＶＩＬ及びアナログ比較器１０４Ａに与える比較電圧ＶＯＨ，ＶＯＬの各電圧値がストアされ、その各電圧値がＤＡ変換器１１１Ｅに与えられ、ＤＡ変換器１１１Ｅで各アナログの電圧値に変換してドライバ１０３Ａとアナログ比較器１０４Ａに与えられる。また、負荷試験回路１１０を動作させる試験条件もレジスタ群１１１Ｂに取り込まれ、負荷試験時にもレジスタ群１１１Ｂに取り込まれたデータが用いられる。

【００２１】レジスタ群１１１Ｃには直流試験時に直流試験に必要な制御信号、例えば、直流試験のモード（電圧印加電流測定モード／電流印加電圧測定モード）印加電圧電流値の設定、測定レンジの設定、クランプ値の設定、測定のスタート、ストップ等を制御すると共に、直流試験の試験結果を格納する。この試験結果は必要に応じて直列信号送受信回路１１１Ａを通じて電気－光変換器Ｅ０１で光信号ＴＸに変換されてメインフレーム２００に伝送される。

【００２２】レジスタ群１１１Ｄにはリレーマトリックス１０５を制御する制御信号がストアされ、この制御信号をリレー制御回路１１１Ｆに入力してリレーマトリックス１０５を制御し、試験モードに対応した切替状態に制御する。つまり、動作試験時はドライバ１０３Ａ及びアナログ比較器１０４Ａを被試験集積回路デバイスＤＵＴの端子Ｐに接続し、直流試験ユニット１１２を切り離す。また、直流試験時はピンエレクトロニクス１０２Ａを切離し、代わって直流試験ユニット１１２を端子Ｐに接続する制御を行う。

【００２３】このようにして、ローカルピンコントローラ１１１は試験モードに応じて各端子Ｐごとに設定すべき条件をレジスタ群１１１Ｂ，１１１Ｃ，１１１Ｄに設定する。レジスタ群１１１Ｂ，１１１Ｃ，１１１Ｄに取り込まれるデータは光の直列信号ＲＸで送られてくるから、その伝送路は１本の光ファイバＯＰＦ１でよく、この光ファイバＯＰＦ１を通じて送られて来た光信号ＲＸは光－電気変換器ＯＥ１で電気信号に変換され、直列信号送受信回路１１１Ａに入力される。なお、この例ではレジスタ群１１１Ｂ，１１１Ｃ，１１１Ｄに取り込まれた各設定データは必要に応じて読み出されて電気－光変換器ＥＯＩで光信号ＴＸに変換され、その光信号ＴＸを光ファイバＯＰＦ２を通じてメインフレームに返送し、メインフレーム側で正しく設定されたか否かを照合できるように構成した場合を示す。

【００２４】光ファイバＯＰＦ３はパターン信号伝送路を構成し、このパターン信号伝送路を通じて端子Ｐに与

えるパターン信号が光信号ＰＡＴで送られてくる。このパターン信号ＰＡＴを光－電気変換器ＯＥ２で電気信号に変換し、ピンエレクトロニクス１０２Ａに搭載しているドライバ１０３Ａに与え、ドライバ１０３Ａから端子Ｐに与えられる。

【００２５】光ファイバＯＰＥ４には機能試験実行時にドライバ１０３Ａの状態を制御するドライバ制御信号ＤＲＥが送られてくる。このドライバ制御信号ＤＲＥによって被試験集積回路デバイスＤＵＴから応答出力を取り出す場合に、ドライバ１０３Ａの出力端子を高インピーダンスの状態に制御し、応答出力信号を有効にアナログ比較器１０４Ａに取り込めるようにしている。

【００２６】光ファイバＯＰＥ５とＯＰＥ６には、アナログ比較器１０４ＡにおいてＨ論理とＬ論理の各レベルを比較するストローブパルスが光信号ＳＴＲＢ－ＨとＳＴＲＢ－Ｌで送られてくる。光信号ＳＴＲＢ－Ｈは被試験デバイスＤＵＴから読出される信号のＨ論理の期間をストローブするためのパルス、光信号ＳＴＲＢ－ＬはＬ論理の期間をストローブするためのパルスである。

【００２７】これらの光ファイバＳＴＲＢ－ＬとＳＴＲＢ－Ｈは光－電気変換器ＯＥ５とＯＥ６で電気信号に変換され、アナログ比較器１１０にストローブパルスとして与える。光ファイバＯＰＦ７とＯＰＦ８はテストヘッド１００からメインフレーム２００にストローブパルスを返送するための伝送路を構成している。この返送されるストローブパルスは実際の回路によりＲ・ＳＴＲＢ－ＨとＲ・ＳＴＲＢ－Ｌはメインフレーム２００からアナログ比較器１０４Ａの間を往復する遅延時間が与えられ、メインフレーム２００に設けられる論理比較器のストローブパルスとして利用される。つまり、光ファイバＯＰＦ７とＯＰＦ８を通じてアナログ比較器１０４Ａの判定結果が光信号に変換されてメインフレームに送られ、論理比較器に入力されるが、その遅延時間とストローブパルスの遅延時間を合致させるためにストローブパルスをメインフレームとテストヘッドの間を往復させている。光ファイバＯＰＦ９とＯＰＦ１０にはアナログ比較器１０４Ａの判定結果つまり、この例では集積回路デバイスＤＵＴの機能試験の試験結果をＳＨ，ＳＬとしてメインフレーム２００に返送する。

【００２８】以上の説明から明らかなように、図１に示した実施例によれば、被試験集積回路デバイスＤＵＴの１端子Ｐごとに１０本の光ファイバでメインフレーム２００とテストヘッド１００との間の信号の授受を実現することができる。直径が比較的太い、例えば５００μｍφのプラスチック光ファイバを用いたとしても、１０本の光ファイバを束ねてもわずかな直径でしかなく、１０００端子分としても10,０００本の光ファイバの束は電気ケーブルのケーブル群３００（図９参照）より充分細いケーブル束となる。

【００２９】図２は図１に示した各部の要素を１端子ごとにユニット化する場合のピンユニットＰＵＮの構造を示す。ケース内の配線基板に図１で説明したローカルピンコントローラ１１１を構成する集積回路素子と、直流試験ユニットを構成する集積回路素子１１２と、ドライバ１０３Ａ，アナログ比較器１０４Ａ，負荷試験回路１１０を収納したピンエレクトロニクス１０２Ａと、リレーマトリックス１０５と、光入出力モジュール１１３と、電源の供給を受ける電気コネクタ１１４と、パフォマンスボードとの接続切離しを行うコネクタ１１５等を収納して構成される。１１６は放熱ブロックを示す。

【００３０】図３にピンユニットＰＵＮをテストヘッド１００に実装する構造の一例を示す。図３に示す１２１は光－電気複合基板を示す。この光－電気複合基板１２１は例えば図４に示すように、多層化された電気配線板１２２の一方の面に光ファイバ埋込層１２３を有し、この光ファイバ埋込層１２３に埋め込んだ光ファイバＯＰＦの端部を４５°に切断し、その切断面Ｓ１を電気配線板１２２の向きに配置して光ファイバＯＰＦを伝達してくる光を配線板の板面と直交する方向に反射させるように構成し、その反射方向にピンユニットＰＵＮに装着した光入出力モジュール１１３を配置させて光ファイバＯＰＦとピンユニットＰＵＮの光入出力モジュール１１３とを光学的に結合させる。

【００３１】光ファイバＯＰＦの他端は配線板の端面に露出させ、この露出面Ｓ２にメインフレーム２００（図３には特に図示しない）から延長されて来た光ファイバケーブル１２４（図３参照）を光学的に結合させることにより、メインフレーム２００とテストヘッド１００側に設けるピンユニットＰＵＮとの間を光伝送路によって接続することができる。なお、ピンユニットＰＵＮに設けた電気コネクタ１１４に関しては通常の電気接続構造によって電気配線板１２２と電気的に接続され、電気配線板１２２を通じてメインフレーム２００に接続される。

【００３２】図３に示す１２５はメインフレーム２００から延長された電源供給用の電気ケーブル、１２６は光－電気複合基板１２１の板面に設けた光結合部、１２７は電気コネクタを示す。これら光結合部１２６と電気コネクタ１２７にピンユニットＰＵＮを設けた光入出力モジュール１１３と電気コネクタ１１４を接続してピンユニットＰＵＮをメインフレーム２００に接続する。

【００３３】光－電気複合基板１２１の板面には光結合部１２６と電気コネクタ１２７を多数配置し、所望の数のピンユニットＰＵＮを実装できるように構成する。

尚、上述ではピンユニットＰＵＮと光ファイバケーブル１２４との接続に光－電気複合基板１２１を用いた例を説明したが必ずしも光－電気複合基板１２１を用いなくても、電気配線板の板面に光コネクタを実装してピンユニットＰＵＮと光ファイバケーブル１２４との接続を行う構造としてもよい。また配線板を用いることなく、光

ファイバケーブル１２４と電気ケーブル１２５の端部に光コネクタ及び電気コネクタを接続し、光ファイバケーブル１２４と電気ケーブル１２５を直接ピンユニットＰＵＮに接続する構造とすることもできる。

【００３４】図３に示す１２８はピンユニットＰＵＮを機械的に支持すると共に、ピンユニットＰＵＮを冷却する機能を持つ冷却フレームを示す。この冷却フレーム１２８は多数のユニット収納孔１２８Ａを有する。ユニット収納孔１２８Ａの周面を囲む壁は、例えば二重構造とされ、内部を冷却水が流通できるように構成する。１２８Ｂと１２８Ｃは冷却水の供給口及び排出口を示す。

【００３５】ピンユニットＰＵＮの上端面には電気コネクタ１１５が設けられ、この電気コネクタ１１５によりピンユニットＰＵＮをパフォーマンスボード１０１に電気的に接続する。なお、図３の例ではパフォーマンスボード１０１の上面に複数台のピンユニットＰＵＮ－Ａを直接搭載し、特に高速素子を試験する場合にこのピンユニットＰＵＮ－Ａを動作させることにより、被試験集積回路デバイスＤＵＴと、ピンユニット間の電気配線を最短状態で接続して試験ができるように構成した場合を示す。

【００３６】図５はテストヘッド１００の他の実施例を示す。この実施例では、光信号伝送路が高速性に優れていることを利用してパターンデータ信号も直列信号で伝送し、テストヘッド１００側で並列信号に戻し、パターンデータ信号を生成するように構成したものである。つまり、この実施例ではローカルピンコントローラ１１１と直流試験ユニット１１２に関しては、図１の実施例と同じであるが、テストパターン信号系に関してテストヘッド１００側に波形整形回路と論理比較回路及びタイミング発生器の一部の機能をメインフレーム側から移設した構造としたものである。

【００３７】つまり、ローカルピンコントローラ１１１と直流試験ユニット１１２の外に波形制御器１３０を設け、この波形制御器１３０によってパターン信号の発生と論理比較動作を行わせるように構成したものである。このため波形制御器１３０にも直列信号送受信回路１３１が設けられ、この直列信号送受信回路１３１によってパターン発生器２０１から送られて来るパターンデータＰＡＴＤＡＴの直列信号を光ファイバＯＰＦ６から受信し、並列信号に変換して波形整形回路１３２に与え、波形整形回路１３２でアナログ波形を持つパターン信号を生成させる。

【００３８】タイミング発生器１３３は図７で説明した微遅延回路ＤＹ２の構成だけをテストヘッド側に移設した場合を示す。つまり、微遅延回路ＤＹ２だけをテストヘッド１００側に移設することにより、テストヘッド１００に移設するタイミング発生器の回路規模を小さく、テストヘッド１００の大形化を避けた構造としたものである。従って、この例ではメインフレーム２００側で粗遅延回路ＤＹ１によってクロックＣＬＫの周期を単位とする粗遅延が与えられたレートパルスＲＡＴが光信号で出力され、このレートパルスＲＡＴが光ファイバＯＰＦ４を通じて送られて来るものとする。この光信号が光－電気変換器ＯＥ３でレートパルスＲＡＴＥに変換され、この電気レートパルスＲＡＴＥをタイミング発生器１３３に与え、このタイミング発生器１３３で微遅延が与えられ、各部のタイミング信号として配分される。微遅延データＴＭＦＩＮは光ファイバＯＰＦ５から直列信号送受信回路１３１を通じてタイミングコントローラ１３５に入力され、タイミングコントローラ１３５によりタイミング発生器１３３が制御される。

【００３９】論理比較回路１３４では波形整形回路１３２に入力されるパターンデータＰＡＴＤＡＴ（ディジタル信号）と被試験集積回路デバイスが出力する応答信号とを論理比較し、その比較結果をフェイル信号ＦＤＡＴとして直列信号送受信回路１３１に送り、直列信号送受信回路１３１から電気－光変換器ＯＥ５に与えられ、光信号に変換して光ファイバＯＰＦ７に送り出される。

【００４０】図６はこの発明の更に他の実施例を示す。この実施例では波形制御器１３０に付随してタイミングメモリＴＭと、パターンメモリＰＭと、フェイルメモリＦＭとを設け、テストヘッド１００側でパターン信号の発生を行わせるように構成した場合を示す。つまり、パターンメモリＰＭには被試験集積回路デバイスＤＵＴの１つの端子Ｐに与えるパターンデータを予め直列信号で光ファイバＯＰＦ５を通じてテストヘッド１００に送り込み記憶させる。更に、そのパターンデータと共にタイミングデータも直列信号ＲＸＸの一部の時間を利用して光ファイバＯＰＦ５を通じてタイミングメモリＴＭに送り込んで記憶させる。従って、試験開始前に全端子分のデータをメインフレーム２００側からテストヘッド１００に設けた各ピンユニットＰＵＮに送り込んで記憶させる。

【００４１】テスト開始と共にパターンメモリＰＭからパターンデータを読み出し、そのパターンデータを波形整形回路１３２でアナログ波形を持つパターン信号に変換する。また、タイミングメモリＴＭも同時に読出され、タイミング発生器１３３でテスト周期を表すレート信号ＲＡＴＥを遅延させて各種のタイミング信号を発生させ、そのタイミング信号を波形整形回路１３２，アナログ比較器１０４Ａ，論理比較器１３４等に分配し、各比較動作のタイミング、パターン信号の立上り、立下りのタイミング等を規定する。

【００４２】論理比較器１３４で不一致が発生するごとに、フェイルメモリＦＭの不良発生アドレスに不良を表す例えばＨ論理の信号を書き込む。フェイルメモリＦＭに取り込まれたフェイルデータ（試験結果）は試験中の空き時間を利用するか、または試験終了時にメモリバスＭＢＵＳと、直列信号送受信回路１３１を通じて電気－

光変換器ＥＯ２で光信号ＴＸＸに変換され、光ファイバＯＰＦ６を通じてメインフレーム２００に送られる。

【００４３】

【発明の効果】以上説明したように、この発明によればメインフレーム２００とテストヘッド１００との間で授受するデータ乃至クロック等の信号は全て光ファイバによって伝送する構成としたから、光ファイバの直径は太いものでも５００μｍ φ程度であり、電気ケーブルより充分細い。従って、仮に光ファイバの本数が従来の電気ケーブルと同数であっても光ケーブルの束の直径は小さい。また光ファイバは電線より軽いから、光ケーブルを束にしても重量は軽く、取扱いは容易である。

【００４４】更に、図５または図６に示したように、直列信号送受信回路１１１Ａ及び１３１を用いることにより、光ケーブルの本数を少なくすることができる。特に図６に示したようにパターンメモリＰＭ，タイミングメモリＴＭ，フェイルメモリＦＭを設けることにより、各種の信号を共通の光ファイバで伝送させることができる。よって、図６に示すように光ファイバの本数を１端子当たり６本程度に少なくすることができる利点が得られる。この結果、メインフレーム２００とテストヘッド１００との間を接続するケーブル群３００の直径を小さくすることができる利点が得られる。

【００４５】また、光ファイバは減衰が少ない特性を持ち、更に相互に光が漏れないことから、メインフレーム２００とテストヘッド１００との距離を離すことができる。従って、例えば発熱量が大きいメインフレーム２００をテストヘッド１００とは別の室に設置することができ、テストヘッド１００だけを例えばクリーンルームに設置する等の配置を採ることができる利点が得られる。また、光信号で信号の授受を行なうから、信号伝送路に終端抵抗を設ける必要がない。よって発熱量の少ない試＊験装置を構成できる利点も得られる。

【図面の簡単な説明】

【図１】この発明の一実施例を説明するためのブロック図。

【図２】図１に示した実施例で用いたピンユニットの構造の一例を説明するための斜視図。

【図３】図２に示したピンユニットを実装する構造の一例を説明するための斜視図。

【図４】図３に示した光－電気複合基板の一例を説明するための断面図。

【図５】この発明の他の実施例を説明するためのブロック図。

【図６】この発明の更に他の実施例を説明するためのブロック図。

【図７】従来の技術を説明するためのブロック図。

【図８】従来の技術の動作を説明するための波形図。

【図９】従来の技術を説明するための斜視図。

【符号の説明】

１００　テストヘッド
ＰＵＮ　ピンユニット
１１１　ローカルピンコントローラ
１１１Ａ，１３１　直列信号送受信回路
１１１Ｂ～１１１Ｄ　レジスタ群
１１１Ｆ　リレー制御回路
１１２　テストヘッドに設けた直流試験ユニット
１１３　光入出力モジュール
１３０　波形制御器
１３２　波形整形回路
１３３　タイミング発生器
１３４　論理比較回路
１３５　タイミングトローラ
１３６　メモリバスコントローラ

【図２】

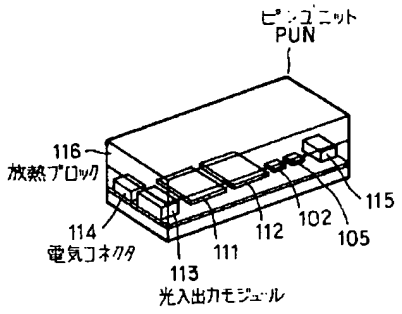


図２

【図８】

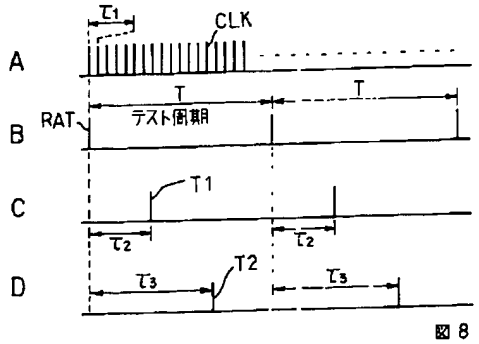


図８

【図１】

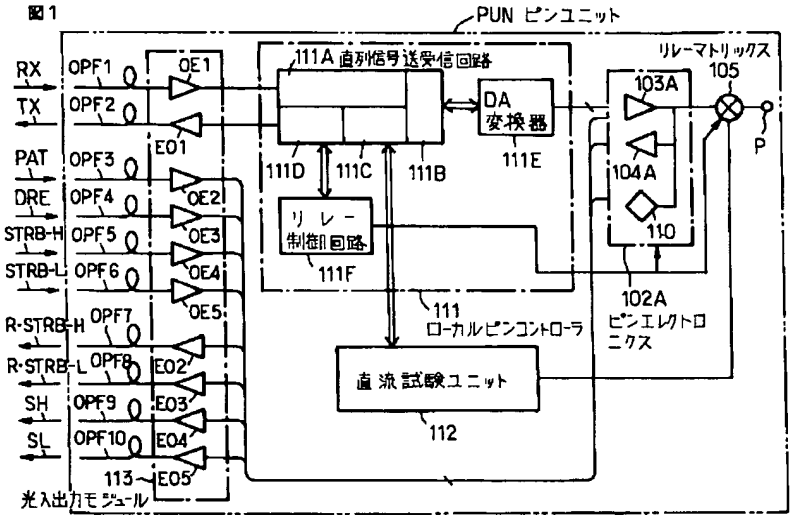


図1
PUN ピンユニット
RX
TX
PAT
DRE
STRB-H
STRB-L
R-STRB-H
R-STRB-L
SH
SL
OPF1
OPF2
OPF3
OPF4
OPF5
OPF6
OPF7
OPF8
OPF9
OPF10
OE1
EO1
OE2
EO2
OE3
EO3
OE4
EO4
OE5
EO5
113
光入出力モジュール
111A 直列信号送受信回路
DA 変換器
111E
111D
111C
111B
リレー制御回路
111F
111
ローカルピンコントローラ
直流試験ユニット
112
リレーマトリックス
105
103A
104A
110
102A
ピンエレクトロニクス
P

【図３】

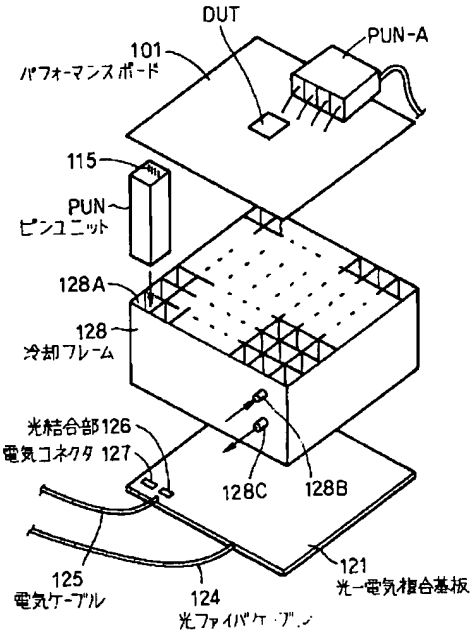

DUT
PUN-A
101
パフォーマンスボード
115
PUN
ピンユニット
128A
128
冷却フレーム
光結合部126
電気コネクタ 127
128C
128B
125
電気ケーブル
124
121
光一電気複合基板

図３

【図９】

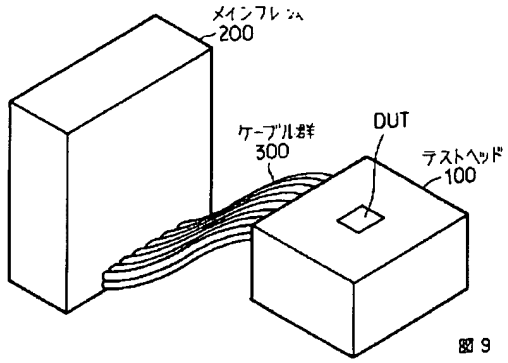

メインフレーム
200
ケーブル群
300
DUT
テストヘッド
100

図９

【図４】

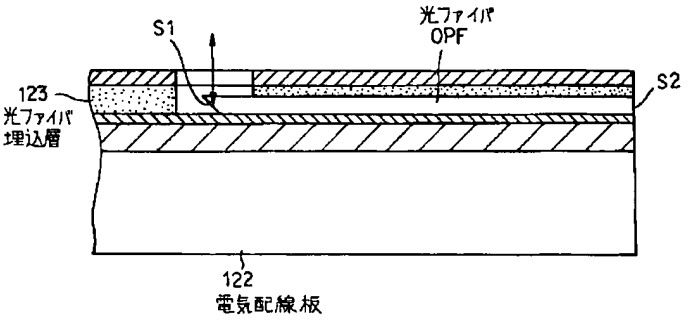

S1
光ファイバ
OPF
S2
123
光ファイバ
埋込層
122
電気配線板

図４

【図５】

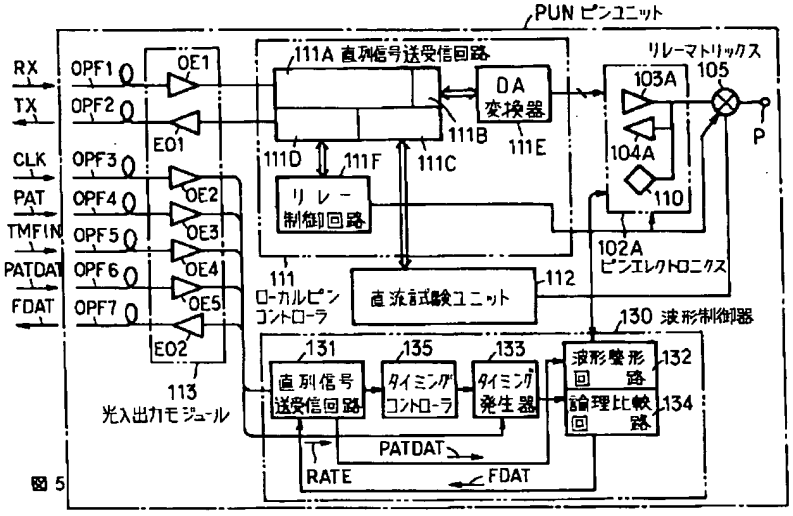
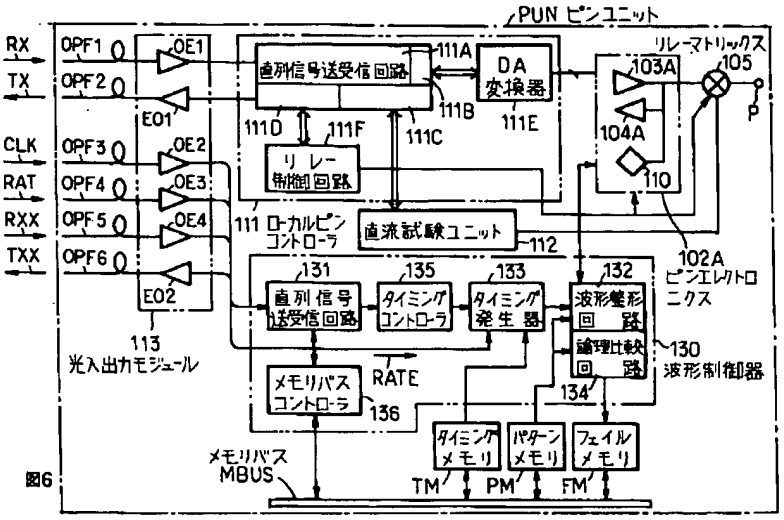
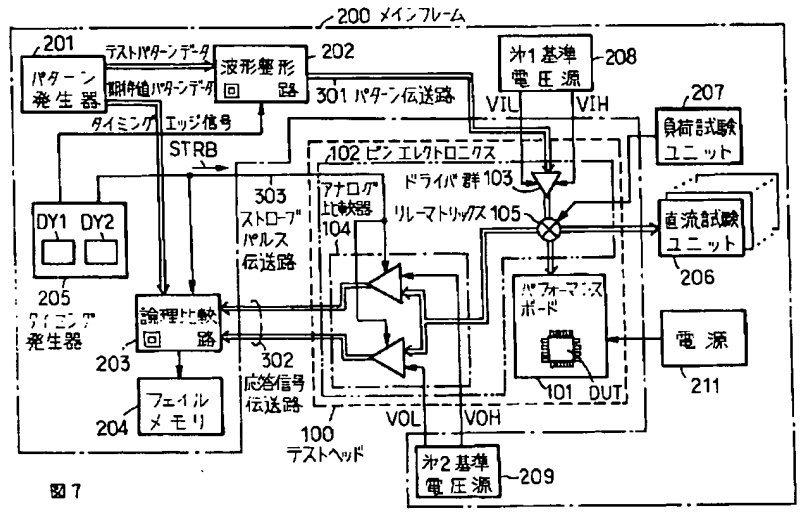

PUN ピンユニット
RX
TX
CLK
PAT
TMFIN
PATDAT
FDAT
OPF1
OPF2
OPF3
OPF4
OPF5
OPF6
OPF7
OE1
EO1
OE2
OE3
OE4
OE5
EO2
113
光入出力モジュール
111A 直列信号送受信回路
DA
変換器
111B
111C
111D
111E
111F
リレー
制御回路
111
ローカルピン
コントローラ
直流試験ユニット
112
リレーマトリックス
103A
104A
105
110
P
102A
ピンエレクトロニクス
130 波形制御器
131
直列信号
送受信回路
135
タイミング
コントローラ
133
タイミング
発生器
波形整形
回路
132
論理比較
回路
134
PATDAT
RATE
FDAT

図５

【図６】


PUN ピンユニット
RX
TX
CLK
RAT
RXX
TXX
OPF1
OPF2
OPF3
OPF4
OPF5
OPF6
OE1
OE2
OE3
OE4
OE01
OE02
113
光入出力モジュール
直列信号送受信回路
111A
111B
111C
111D
111F
DA
変換器
111E
リレー
制御回路
111 ローカルピン
コントローラ
直流試験ユニット
112
リレーマトリックス
103A
105
104A
110
P
102A
ピンエレクトロニクス
131
直列信号
送受信回路
135
タイミング
コントローラ
133
タイミング
発生器
132
波形整形
回路
論理比較
回路
130
波形制御器
134
メモリバス
コントローラ
136
RATE
メモリバス
MBUS
タイミング
メモリ
パターン
メモリ
フェイル
メモリ
TM
PM
FM
図6

【図７】


200 メインフレーム
201
パターン
発生器
テストパターンデータ
期待値パターンデータ
タイミングエッジ信号
STRB
波形整形
回路
202
301 パターン伝送路
沖1基準
電圧源
208
VIL
VIH
207
負荷試験
ユニット
102 ピンエレクトロニクス
ドライバ群 103
リレーマトリックス 105
303
ストローブ
パルス
伝送路
アナログ
比較器
104
直流試験
ユニット
206
DY1 DY2
205
タイミング
発生器
論理比較
回路
203
302
応答信号
伝送路
パフォーマンス
ボード
101 DUT
電源
211
フェイル
メモリ
204
100
テストヘッド
VOL
VOH
沖2基準
電圧源
209
図7

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The integrated-circuit device testing device characterized by constituting all or some of signal-transmission way between the above-mentioned main frame and a test head by the lightwave signal way in the integrated-circuit device testing device constituted by providing the main frame which stored the pattern generator, and the test head which it is separated and installed from this main frame, and an examined device is contacted, and performs that trial.
[Claim 2] The integrated-circuit device testing device characterized by constituting so that may transmit the data which are sent into a test head from the above-mentioned main frame, and which are set up for every terminal by the serial signal of light in an integrated-circuit device testing device according to claim 1, it may receive in the serial transceiver circuit established in the test head side, it may change into a parallel signal and it may store in a register group.
[Claim 3] The integrated-circuit device testing device characterized by considering as the configuration which sets they to be [any of an integrated-circuit device testing device according to claim 1 or 2], prepares a direct-current trial unit in a test head side, transmits the control signal to this direct-current trial unit by the serial signal of light from a main frame side, controls a direct-current trial unit, and performs the direct-current trial of an examined device.
[Claim 4] The integrated-circuit device testing device characterized by constituting so that the setting data and a direct-current test result may be transmitted to a mainframe as a serial signal of light in the above-mentioned serial transceiver circuit while storing the data and the direct-current test result which are set up for every terminal in the register group by the side of a test head in the integrated-circuit device testing device according to claim 3.
[Claim 5] In an integrated-circuit device testing device according to claim 4, the pattern signal given to an examined device is supplied to a test head from a mainframe as a serial signal of light for every terminal. While giving an examined device through the driver prepared in the test head It judges whether it has H logic electrical potential difference and L logic electrical potential difference of normal with the analog comparator which was read from the examined device and which read and formed the signal in the test head. The integrated-circuit device testing device characterized by considering as the configuration which changes the judgment result into the serial signal of light with electric - phototransducer for every terminal, and is transmitted to a main frame through an optical transmission line.
[Claim 6] In an integrated-circuit testing device according to claim 3, the 2nd serial signal transceiver circuit, a waveform shaping circuit, and a logic comparator are prepared in a test head corresponding to each terminal of an examined device. Digital pattern data are transmitted to a test head by the serial signal of light for every terminal from a main frame. In a test head, receive in the above-mentioned 2nd serial signal transceiver circuit, and it changes into juxtaposition pattern data. While changing this juxtaposition pattern data into the pattern signal of an analog in the above-mentioned waveform shaping circuit and giving this pattern signal to each terminal of an examined device through a driver It judges whether logical level is normal in the read-out signal of an examined device at an analog comparator.

Logical comparison is carried out to the digital expectation value pattern data with which the judgment result is sent from a main frame by the logic comparator. The integrated-circuit device testing device characterized by considering as the configuration which transmits the logical-comparison result to a main frame as a serial signal of light through the above-mentioned 2nd serial signal transceiver circuit.
[Claim 7] The integrated-circuit device testing device characterized by to consider as the configuration which controls actuation of the above-mentioned waveform shaping circuit, a logical-comparison circuit, and an analog comparator circuit according to the timing signal which prepares a timing generator in a test head, changes and gives the digital timing data transmitted to this timing generator by the serial signal of light from the main frame to a parallel signal in an integrated-circuit device testing device according to claim 6 in the above-mentioned 2nd serial signal transceiver circuit, and is outputted from a timing generator.
[Claim 8] In an integrated-circuit device testing device according to claim 7 to a test head Pattern memory, Prepare fail memory and timing memory and pattern memory and timing memory are made to transmit and memorize pattern data and timing data with a lightwave signal beforehand from a main frame. With experimental initiation While reading pattern data and timing data from such memory, generating a pattern signal and a timing signal in a waveform shaping circuit and a timing generator and performing the functional test of an examined device The integrated-circuit device testing device characterized by obtaining the result of a functional test from a logical-comparison circuit, making the above-mentioned fail memory memorize this test result, and transmitting that storage to a main frame with a lightwave signal.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the integrated-circuit device testing device which examines a semiconductor integrated circuit device (IC) or a large-scale-integrated-circuit device (LSI).
[0002]
[Description of the Prior Art] The configuration of the outline of the common integrated-circuit device testing device to drawing 7 is shown. The part to which 100 in drawing is called a test head, and 200 is called a mainframe is shown, respectively. A performance board 101 and pin electronics 102 are carried in a test head 100. It is equipped with the socket which contacts the examined device DUT in a performance board 101, and the examined device DUT and a testing device are electrically connected through this socket (not shown especially in drawing).
[0003] The relay matrix 105 which changes the analog comparator group 104 which judges whether H logic and L logic of a responded-output signal which are read from the examined device DUT have the electrical-potential-difference value of normal to be the driver group 103 which generally drives the examined device DUT electrically, and the equipment group linked to each terminal of the examined device DUT is stored in pin electronics 102.
[0004] A pattern generator 201 is formed in a mainframe 200, and test pattern data (digital signal) are outputted from this pattern generator 201. This test pattern data and a timing edge signal are inputted into a waveform shaping circuit 202, and the pattern signal (signal with an analog wave) given to each terminal of the examined device DUT in this waveform shaping circuit 202 is made to generate. This pattern signal is sent out to a test head 100 through the pattern transmission line 301, and is given to each terminal of the examined device DUT through the driver group 103. In addition, a timing signal is also transmitted to coincidence in this pattern transmission line 301.
[0005] The comparison result of the analog comparator group 104 is returned to a mainframe 200 through the reply signal transmission line 302, carries out logical comparison to the expectation value pattern which a pattern generator 201 generates in the logical-comparison circuit 203, detects generating of an inequality, and detects a defect part. 204 shows fail memory, and whenever an inequality occurs in the logical-comparison circuit 203, it writes in for example, H logic which expresses a defect with the address which the defect generated.
[0006] 205 shows a timing generator. Existence of the coarse-delay circuit DY1 and the fine delay circuit DY2 is beforehand explained for the sake of the convenience explaining separating into a mainframe 200 and a test head 100, and installing the coarse-delay circuit DY1 and the fine delay circuit DY2 by this invention, behind, about this timing generator 205. Conventionally, in a timing generator 205, while acquiring the rate pulse RAT (drawing 8 B) which carries out dividing of the reference clock CLK shown in drawing 8 A, and determines the test period T, arbitration carries out time delay of this rate pulse RAT, and the timing of the wave-like standup of various kinds of timing signals, for example, a test pattern signal, the timing of falling, the timing of the strobe of the analog comparator group 104, the timing of comparison actuation of the logical-comparison circuit 203, etc. are generated.

[0007] Therefore, many delay circuits which arbitration can make carry out time delay of the rate pulse RAT to a timing generator 205 in within the limits of the test period TK or the several times as many range as this are prepared, and the timing signals T1 and T2 of various kinds as shown, for example in drawing 8 C and D in which arbitration carried out time delay from criteria timing by the delay circuit of these large number are made to generate.
[0008] Many delay circuits established in a timing generator 205 carry out counting of the clock CLK, and are the periods tau 1 of Clock CLK. The coarse-delay circuit DY1 which gives the time delay made into a unit, and period tau 1 of Clock CLK It was constituted by the combination of the fine delay circuit DY2 which divides within the limits still more finely and specifies a time delay, for example, picosecond resolution-of-the-identity ability has prescribed the standup of a test pattern signal, the timing of falling, etc.
[0009] In addition to this, the direct-current trial unit 206, the source 208 of the 1st reference voltage which sets up the load test unit 207 and the electrical-potential-difference values VIH and VIL of H logic of a pattern signal and L logic, the source 209 of the 2nd reference voltage which gives the comparison electrical potential differences VOH and VOL to the analog comparator group 104, and the power unit 211 which gives the electrical potential difference for operating the examined device DUT are formed in a mainframe 200.
[0010]
[Problem(s) to be Solved by the Invention] The connection situation of a test head 100 and a mainframe 200 is shown in drawing 9 . It connects by the cable group 300 between a main frame 200 and a test head 100. Since various kinds of signal lines exist between a mainframe 200 and a test head 100 as drawing 7 explained, the number of the cable contained by the cable group 300 increases.
[0011] Moreover, it is in the inclination which the number of terminals of a device increases with improvement in the degree of integration of a semiconductor integrated circuit device. Furthermore, improvement in a working speed and the number of the cable of the cable group 300 which connects between a main frame 200 and test heads 100 for a certain reason are in the inclination of an increment. for example, in a testing device with the test capacity for 1000 terminals The number of the signals delivered and received between a mainframe 200 and a test head 100 attains to tens of thousands of numbers. Rapidity, high degree of accuracy, noise-proof nature, etc. are taken into consideration to each. And a twisted pair, since special cables, such as a coaxial cable and multiplex shielding, are used -- a substantial conductor -- a number will be several times the number of signals, and the cable group 300 serves as a huge bundle, and makes difficult migration of a test head 100, such as etc., anchoring of a handler -- demounting.
[0012] Moreover, if the cable group 300 is lengthened, the cross talk between cables will also increase, and there is also un-arranging [which degrades trial precision]. Furthermore, since large power is needed for transmitting these signals of a lot of, this means the increment in calorific value, and makes cooling difficult and the number of terminator machines also increases, it is the factor which checks the miniaturization of a system.
[0013] The purpose of this invention tends to offer the integrated-circuit device testing device which can also suppress generating of the cross talk between signals while it minimum-izes the cable group which connects between a main frame and test heads and makes the handling of a test head easy.
[0014]
[Means for Solving the Problem] All or some of signal-transmission way between a mainframe and a test head is transposed to the lightwave signal transmission line suitable for high-speed transmission, and it constitutes from this invention so that the signal between a mainframe and a test head may be made to deliver and receive with a lightwave signal. The data or the various timing signals which are sent into a test head from a main frame in this invention and which are set up for every terminal are transmitted by the serial signal of light, the serial receiving means formed in the test head side receives, and while changing into a parallel signal and storing in a setting register, measurement data and the integrated-circuit device testing device which considered the measurement result as the configuration returned with a lightwave signal are offered.

[0015] Pattern memory and a waveform shaping circuit are further established in a test head side, the digital test pattern data which a pattern generator outputs are transmitted to a test head by the serial signal of light, and pattern memory is made to memorize in this invention. With test initiation, the test pattern data memorized in this pattern memory are read, it changes into the pattern signal of an analog in that test pattern data (digital signal) and waveform shaping circuit that were read, and the integrated-circuit device testing device constituted so that this pattern signal might be impressed to the examined device DUT through a driver group is offered.
[0016] since that diameter is 200 - 500micrometer phi extent and does not need a go and return conductor for every channel like an electrical signal, even if a lightwave signal transmission line uses a plastic optical fiber according to the configuration of this invention -- the gestalt of a signal-transmission way -- minor-diameter-izing -- and it can lightweight-ize. Since the number of an optical fiber can be lessened by considering as the configuration delivered and received especially by the serial signal of light, the path of a cable group can be further made small and lightweight-ization can also be attained. Moreover, an optical fiber does not have generating of a cross talk mutually, in order that light may transmit only a part for a core. Therefore, the advantage which can lengthen extended distance is also acquired.
[0017]
[Embodiment of the Invention] One example of this invention is shown in drawing 1 . Drawing shows the configuration of the part (this part is called the pin unit PUN below) which carries out the analog comparison of the signal which supplied the pattern signal to one terminal by the side of a test head 100 (one terminal P of the examined device DUT), and was outputted from this terminal, and is sent to a mainframe 200.
[0018] In addition to the relay matrix 105, in this example, the cases where the local pin controller 111, the direct-current trial unit 112, and the optical input/output module 113 are formed are indicated to be driver 103A which drives one terminal P of the examined integrated-circuit device DUT and analog comparator 104A, and pin electronics 102A which carried the load test circuit 110 to the pin unit PUN.
[0019] The optical input/output module 113 has photoelectric transducers OE1-OE5, and the electrical and electric equipment and phototransducers EO1-EO5, changes into an electrical signal the lightwave signal sent from a mainframe 200 by light and the electrical-potential-difference converters OE1-OE5, and performs a functional test and a direct-current trial using the electrical signal. Serial signal transceiver circuit 111A which receives the serial signal with which the local pin controller 111 is sent through light and the electrical-potential-difference converter OE1 from an optical fiber OPF1, With the register groups 111B, 111C, and 111D which incorporate various kinds of setting data received by this serial signal transceiver circuit 111A, and the setting data incorporated to register group 111B For example, DA converter 111E which generates the comparison electrical potential differences VOH and VOL given to the electrical potential differences VIH and VIL and analog comparator 104A which are given to driver 103A, Relay control circuit 111F which control the condition of the relay matrix 105 by the relay control signal incorporated to register group 111D can be provided and constituted.
[0020] That is, each electrical-potential-difference value of the comparison electrical potential differences VOH and VOL given to the electrical potential difference VIH of H logic, the electrical potential difference VIL of L logic, and analog comparator 104A which are given to driver 103A is stored in register group 111B, and it is given to DA converter 111E, and each of that electrical-potential-difference value changes into the electrical-potential-difference value of each analog by DA converter 111E, and is given to driver 103A and analog comparator 104A. Moreover, the data with which the test condition which operates the load test circuit 110 was also incorporated by register group 111B, and was incorporated by register group 111B also at the time of a load test are used.
[0021] While controlling the start of a setup of a control signal required for a direct-current trial, for example, the mode (voltage-source-current-measurement mode / current-source-voltage-measurement mode) applied-voltage current value of a direct-current trial, a setup of a measurement range, a setup of a clamp value, and measurement, a stop, etc. to register group 111C at the time of a direct-current trial, the test result of a direct-current trial is stored. This test result is changed into a lightwave signal TX

with the electric-phototransducer E01 through serial signal transceiver circuit 111A if needed, and is transmitted to a mainframe 200.
[0022] The control signal which controls the relay matrix 105 is stored in register group 111D, this control signal is inputted into relay control circuit 111F, the relay matrix 105 is controlled, and it controls in the change condition corresponding to test mode. That is, driver 103A and analog comparator 104A are connected to the terminal P of the examined integrated-circuit device DUT at the time of a performance test, and it separates the direct-current trial unit 112. Moreover, control which detaches pin electronics 102A and instead connects the direct-current trial unit 112 to Terminal P is performed at the time of a direct-current trial.
[0023] Thus, the local pin controller 111 sets the conditions which should be set to each terminal P of every according to test mode as the register groups 111B, 111C, and 111D. Since the data incorporated by the register groups 111B, 111C, and 111D are sent by the serial signal RX of light, one optical fiber OPF1 is sufficient as that transmission line, and the lightwave signal RX sent through this optical fiber OPF1 is changed into an electrical signal by the photoelectric transducer OE1, and is inputted into serial signal transceiver circuit 111A. In addition, in this example, each setting data incorporated by the register groups 111B, 111C, and 111D is read if needed, and is changed into a lightwave signal TX with the electric - phototransducer EOI, that lightwave signal TX is returned to a mainframe through an optical fiber OPF2, and the case where it constitutes so that it can collate whether it was correctly set up by the mainframe side is shown.
[0024] An optical fiber OPF3 constitutes a pattern signal-transmission way, and the pattern signal given to Terminal P through this pattern signal-transmission way is sent with a lightwave signal PAT. This pattern signal PAT is changed into an electrical signal by the photoelectric transducer OE2, it gives driver 103A carried in pin electronics 102A, and Terminal P is given from driver 103A.
[0025] The driver control signal DRE which controls the condition of driver 103A at the time of functional test activation is sent to an optical fiber OPE4. When taking out responded output from the examined integrated-circuit device DUT with this driver control signal DRE, the output terminal of driver 103A is controlled in the condition of a high impedance, and it enables it to incorporate a responded-output signal to analog comparator 104A effectively.
[0026] The strobe pulse which compares each level of H logic and L logic in analog comparator 104A is sent to optical fibers OPE5 and OPE6 by lightwave signal STRB-H and STRB-L. A pulse for lightwave signal STRB-H to carry out the strobe of the period of H logic of the signal read from the examined device DUT and lightwave signal STRB-L are the pulses for carrying out the strobe of the period of L logic.
[0027] These optical fiber STRB-L and STRB-H are changed into an electrical signal by photoelectric transducers OE5 and OE6, and are given to an analog comparator 110 as a strobe pulse. Optical fibers OPF7 and OPF8 constitute the transmission line for returning a strobe pulse to a main frame 200 from a test head 100. The time delay to which R-STRB-H and R-STRB-L go back and forth between analog comparator 104A from a mainframe 200 is given by the circuit where this strobe pulse returned is actual, and is used as a strobe pulse of the logic comparator prepared in a mainframe 200. That is, in order to make the time delay and time delay of a strobe pulse agree, the strobe pulse is made to go back and forth between a main frame and test heads, although the judgment result of analog comparator 104A is changed into a lightwave signal through optical fibers OPF7 and OPF8, it is sent to a main frame and it is inputted into a logic comparator. The test result of the functional test of the integrated-circuit device DUT is returned to a mainframe 200 as SH and SL at optical fibers OPF9 and OPF10, the judgment result, i.e., this example, of analog comparator 104A.
[0028] According to the example shown in drawing 1 , transfer of the signal between a mainframe 200 and a test head 100 is realizable for every [of the examined integrated-circuit device DUT] 1 terminal P with ten optical fibers so that clearly from the above explanation. A diameter is comparatively thick, for example, even if it uses the plastic optical fiber of 500micrometer phi, even if it bundles ten optical fibers, it cannot but be few diameters, and becomes a cable bundle with the bundle of 10,000 optical fibers sufficiently thinner than the cable group 300 (refer to drawing 9) of an electrical cable also as a

part for 1000 terminals.
[0029] Drawing 2 shows the structure of the pin unit PUN in the case of carrying out unitization of the element of each part shown in drawing 1 for every terminal. The connector 115 grade which performs connection isolation with the integrated circuit device which constitutes the local pin controller 111 explained by drawing 1 , the integrated circuit device 112 which constitutes a direct-current trial unit, driver 103A, analog comparator 104A and pin electronics 102A that contained the load test circuit 110, the relay matrix 105, the optical input/output module 113, the electrical connector 114 that receives supply of a power source, and a PAFOMANSU board is contained to the wiring substrate within a case, and it is constituted. 116 shows a heat dissipation block.
[0030] An example of structure which mounts the pin unit PUN in a test head 100 at drawing 3 is shown. 121 shown in drawing 3 shows optical-electrical-and-electric-equipment compound substrate. This optical-electrical-and-electric-equipment compound substrate 121 has the optical fiber buried layer 123 in one field of the multilayered electric wiring plate 122, as shown in drawing 4 . The edge of the optical fiber OPF embedded at this optical fiber buried layer 123 is cut at 45 degrees. It constitutes so that the light which arranges the cutting plane S1 to the sense of the electric wiring plate 122, and transmits an optical fiber OPF may be reflected in the direction which intersects perpendicularly with the plate surface of a patchboard. The optical input/output module 113 with which the pin unit PUN was equipped is arranged in the reflective direction, and an optical fiber OPF and the optical input/output module 113 of the pin unit PUN are optically combined with it.
[0031] The other end of an optical fiber OPF can connect between a main frame 200 and the pin units PUN prepared in a test head 100 side by the optical transmission line by making it expose to the end face of a patchboard, and combining optically the fiber optic cable 124 (referring to drawing 3) extended by this exposure S2 from the main frame 200 (not shown to especially drawing 3 R> 3). In addition, about the electrical connector 114 prepared in the pin unit PUN, according to the usual electrical connection structure, it connects with the electric wiring plate 122 electrically, and connects with a mainframe 200 through the electric wiring plate 122.
[0032] The electrical cable for current supply with which 125 shown in drawing 3 was extended from the main frame 200, the optical coupling section which prepared 126 in the plate surface of optical-electrical-and-electric-equipment compound substrate 121, and 127 show an electrical connector. The optical input/output module 113 and electrical connector 114 which formed the pin unit PUN in these optical coupling section 126 and an electrical connector 127 are connected, and the pin unit PUN is connected to a mainframe 200.
[0033] To the plate surface of optical-electrical-and-electric-equipment compound substrate 121, many optical coupling sections 126 and electrical connectors 127 are arranged, and it constitutes so that a desired number of pin units PUN can be mounted. In addition, although the example which used optical-electrical-and-electric-equipment compound substrate 121 for connection between the pin unit PUN and a fiber optic cable 124 in **** was explained, even if it does not necessarily use optical - electrical-and-electric-equipment compound substrate 121, it is good also as structure of mounting an optical connecter in the plate surface of an electric wiring plate, and making connection between the pin unit PUN and a fiber optic cable 124. Moreover, without using a patchboard, an optical connecter and an electrical connector can be connected to the edge of a fiber optic cable 124 and an electrical cable 125, and a fiber optic cable 124 and an electrical cable 125 can also be made into the structure linked to the direct pin unit PUN.
[0034] 128 shown in drawing 3 shows a cooling frame with the function which cools the pin unit PUN while supporting the pin unit PUN mechanically. This cooling frame 128 has much unit receipt hole 128A. The wall surrounding the peripheral surface of unit receipt hole 128A is made into dual structure, and it constitutes the interior so that cooling water can circulate. 128B and 128C show the feed hopper and exhaust port of cooling water.
[0035] An electrical connector 115 is formed in the upper limit side of the pin unit PUN, and the pin unit PUN is electrically connected to a performance board 101 by this electrical connector 115. In addition, in the example of drawing 3 , when two or more sets of pin unit PUN-A are directly carried in the top

face of a performance board 101 and it examines especially a high-speed component, the case where it constitutes so that the electric wiring between pin units may be connected with the examined integrated-circuit device DUT in the state of the shortest and a trial may be possible is shown by operating this pin unit PUN-A.

[0036] Drawing 5 shows other examples of a test head 100. Using the lightwave signal transmission line being excellent in rapidity, a pattern data signal is also transmitted by the serial signal, and it returns to a parallel signal by the test head 100 side, and it constitutes from this example so that a pattern data signal may be generated. That is, in this example, about the local pin controller 111 and the direct-current trial unit 112, although it is the same as the example of drawing 1 , it considers as the structure which transferred the function of some waveform shaping circuits, logical-comparison circuits, and timing generators to the test head 100 side from the mainframe side about the test pattern signal system.

[0037] That is, the wave controller 130 is formed out of the local pin controller 111 and the direct-current trial unit 112, and it constitutes so that this wave controller 130 may be made to perform generating and logical-comparison actuation of a pattern signal. For this reason, the serial signal transceiver circuit 131 is established also in the wave controller 130, the serial signal of the pattern data PATDAT sent by this serial signal transceiver circuit 131 from a pattern generator 201 is received from an optical fiber OPF6, it changes into a parallel signal, a waveform shaping circuit 132 is given, and the pattern signal which has an analog wave in a waveform shaping circuit 132 is made to generate.

[0038] A timing generator 133 shows the case where only the configuration of the fine delay circuit DY2 explained by drawing 7 is transferred to a test head side. That is, by relocating only the fine delay circuit DY2 to a test head 100 side, it is small in the circuit scale of the timing generator transferred to a test head 100, and considers as the structure which avoided large-sized-ization of a test head 100. Therefore, in this example, the rate pulse RAT to which the coarse delay which makes the period of Clock CLK a unit by the coarse-delay circuit DY1 was given by the mainframe 200 side shall be outputted with a lightwave signal, and this rate pulse RAT shall be sent through an optical fiber OPF4. This lightwave signal is changed into the rate pulse RATE by the photoelectric transducer OE3, and this electric rate pulse RATE is given to a timing generator 133, and with this timing generator 133, fine delay is given and it is distributed as a timing signal of each part. Fine lag data TMFIN is inputted into the timing controller 135 through the serial signal transceiver circuit 131 from an optical fiber OPF5, and a timing generator 133 is controlled by the timing controller 135.

[0039] In the logical-comparison circuit 134, logical comparison of the pattern data PATDAT (digital signal) inputted into a waveform shaping circuit 132 and the reply signal which an examined integrated-circuit device outputs is carried out, the comparison result is given by the electric-phototransducer OE5 from delivery and the serial signal transceiver circuit 131 as a fail signal FDAT in the serial signal transceiver circuit 131, and it changes into a lightwave signal, and is sent out to an optical fiber OPF7.

[0040] Drawing 6 shows the example of further others of this invention. In this example, along with the wave controller 130, the timing memory TM, the pattern memory PM, and the fail memory FM are formed, and the case where it constitutes so that a pattern signal may be generated by the test head 100 side is shown. That is, the pattern memory PM is made to send in and memorize beforehand the pattern data given to one terminal P of the examined integrated-circuit device DUT to a test head 100 through an optical fiber OPF5 by the serial signal. Furthermore, the timing memory TM is made to also send in and memorize timing data through an optical fiber OPF5 using a part of time amount of the serial signal RXX with the pattern data. Therefore, each pin unit PUN prepared in the test head 100 is made to send in and memorize the data for all terminals from a mainframe 200 side before test initiation.

[0041] Pattern data are read from the pattern memory PM with test initiation, and the pattern data is changed into the pattern signal which has an analog wave in a waveform shaping circuit 132. Moreover, it is read to coincidence, and rate signal RATE which expresses a test period with a timing generator 133 is delayed, various kinds of timing signals are generated, the timing signal is distributed to a waveform shaping circuit 132, analog comparator 104A, and logic-comparator 134 grade, and the timing memory TM specifies the timing of each comparison actuation, the standup of a pattern signal, the timing of falling, etc.

[0042] Whenever an inequality occurs in a logic comparator 134, the signal of for example, H logic which expresses a defect with the defect generating address of the fail memory FM is written in. The fail data (test result) incorporated by the fail memory FM use the idle time under trial, or are changed into a lightwave signal TXX with the electric - phototransducer EO2 through a memory bus MBUS and the serial signal transceiver circuit 131 at the time of test termination, and are sent to a mainframe 200 through an optical fiber OPF6.

[0043]

[Effect of the Invention] According to this invention, as explained above, since all the signals of the data delivered and received between a main frame 200 and a test head 100 thru/or a clock, etc. were considered as the configuration transmitted with an optical fiber, a thick thing is also 500micrometer phi extent, and an optical numerical aperture's are thinner than an electrical cable enough. Therefore, even if the number of an optical fiber is a conventional electrical cable and the conventional same number, the diameter of the bundle of an optical cable will be small. Moreover, since an optical fiber is lighter than an electric wire, even if it makes an optical cable into a bundle, weight is light, and handling is easy.

[0044] Furthermore, as shown in drawing 5 or drawing 6 , the number of an optical cable can be lessened by using the serial signal transceiver circuits 111A and 131. Various kinds of signals can be made to transmit with a common optical fiber by forming the pattern memory PM, the timing memory TM, and the fail memory FM, as shown especially in drawing 6 . Therefore, the advantage which can lessen the number of an optical fiber about six per one terminal as shown in drawing 6 is acquired. Consequently, the advantage which can make small the diameter of the cable group 300 which connects between a main frame 200 and test heads 100 is acquired.

[0045] Moreover, since attenuation has few properties and light does not leak mutually further, an optical fiber can detach the distance of a mainframe 200 and a test head 100. It can follow, for example, the mainframe 200 with large calorific value can be installed in ** with an another test head 100, and the advantage which can take arrangement of installing only a test head 100 in a clean room is acquired. Moreover, since a signal is delivered and received with a lightwave signal, it is not necessary to prepare a terminator in a signal-transmission way. Therefore, the advantage which can constitute a testing device with little calorific value is also acquired.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the integrated-circuit device testing device which examines a semiconductor integrated circuit device (IC) or a large-scale-integrated-circuit device (LSI).

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PRIOR ART

[Description of the Prior Art] The configuration of the outline of the common integrated-circuit device testing device to drawing 7 is shown. The part to which 100 in drawing is called a test head, and 200 is called a mainframe is shown, respectively. A performance board 101 and pin electronics 102 are carried in a test head 100. It is equipped with the socket which contacts the examined device DUT in a performance board 101, and the examined device DUT and a testing device are electrically connected through this socket (not shown especially in drawing).
[0003] The relay matrix 105 which changes the analog comparator group 104 which judges whether H logic and L logic of a responded-output signal which are read from the examined device DUT have the electrical-potential-difference value of normal to be the driver group 103 which generally drives the examined device DUT electrically, and the equipment group linked to each terminal of the examined device DUT is stored in pin electronics 102.
[0004] A pattern generator 201 is formed in a mainframe 200, and test pattern data (digital signal) are outputted from this pattern generator 201. This test pattern data and a timing edge signal are inputted into a waveform shaping circuit 202, and the pattern signal (signal with an analog wave) given to each terminal of the examined device DUT in this waveform shaping circuit 202 is made to generate. This pattern signal is sent out to a test head 100 through the pattern transmission line 301, and is given to each terminal of the examined device DUT through the driver group 103. In addition, a timing signal is also transmitted to coincidence in this pattern transmission line 301.
[0005] The comparison result of the analog comparator group 104 is returned to a mainframe 200 through the reply signal transmission line 302, carries out logical comparison to the expectation value pattern which a pattern generator 201 generates in the logical-comparison circuit 203, detects generating of an inequality, and detects a defect part. 204 shows fail memory, and whenever an inequality occurs in the logical-comparison circuit 203, it writes in for example, H logic which expresses a defect with the address which the defect generated.
[0006] 205 shows a timing generator. Existence of the coarse-delay circuit DY1 and the fine delay circuit DY2 is beforehand explained for the sake of the convenience explaining separating into a mainframe 200 and a test head 100, and installing the coarse-delay circuit DY1 and the fine delay circuit DY2 by this invention, behind, about this timing generator 205. Conventionally, in a timing generator 205, while acquiring the rate pulse RAT (drawing 8 B) which carries out dividing of the reference clock CLK shown in drawing 8 A, and determines the test period T, arbitration carries out time delay of this rate pulse RAT, and the timing of the wave-like standup of various kinds of timing signals, for example, a test pattern signal, the timing of falling, the timing of the strobe of the analog comparator group 104, the timing of comparison actuation of the logical-comparison circuit 203, etc. are generated.
[0007] Therefore, many delay circuits which arbitration can make carry out time delay of the rate pulse RAT to a timing generator 205 in within the limits of the test period TK or the several times as many range as this are prepared, and the timing signals T1 and T2 of various kinds as shown, for example in drawing 8 C and D in which arbitration carried out time delay from criteria timing by the delay circuit of these large number are made to generate.

[0008] Many delay circuits established in a timing generator 205 carry out counting of the clock CLK, and are the periods tau 1 of Clock CLK. The coarse-delay circuit DY1 which gives the time delay made into a unit, and period tau 1 of Clock CLK It was constituted by the combination of the fine delay circuit DY2 which divides within the limits still more finely and specifies a time delay, for example, picosecond resolution-of-the-identity ability has prescribed the standup of a test pattern signal, the timing of falling, etc.

[0009] In addition to this, the direct-current trial unit 206, the source 208 of the 1st reference voltage which sets up the load test unit 207 and the electrical-potential-difference values VIH and VIL of H logic of a pattern signal and L logic, the source 209 of the 2nd reference voltage which gives the comparison electrical potential differences VOH and VOL to the analog comparator group 104, and the power unit 211 which gives the electrical potential difference for operating the examined device DUT are formed in a mainframe 200.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, as explained above, since all the signals of the data delivered and received between a main frame 200 and a test head 100 thru/or a clock, etc. were considered as the configuration transmitted with an optical fiber, a thick thing is also 500micrometer phi extent, and an optical numerical aperture's are thinner than an electrical cable enough. Therefore, even if the number of an optical fiber is a conventional electrical cable and the conventional same number, the diameter of the bundle of an optical cable will be small. Moreover, since an optical fiber is lighter than an electric wire, even if it makes an optical cable into a bundle, weight is light, and handling is easy.
[0044] Furthermore, as shown in drawing 5 or drawing 6 , the number of an optical cable can be lessened by using the serial signal transceiver circuits 111A and 131. Various kinds of signals can be made to transmit with a common optical fiber by forming the pattern memory PM, the timing memory TM, and the fail memory FM, as shown especially in drawing 6 . Therefore, the advantage which can lessen the number of an optical fiber about six per one terminal as shown in drawing 6 is acquired. Consequently, the advantage which can make small the diameter of the cable group 300 which connects between a main frame 200 and test heads 100 is acquired.
[0045] Moreover, since attenuation has few properties and light does not leak mutually further, an optical fiber can detach the distance of a mainframe 200 and a test head 100. It can follow, for example, the mainframe 200 with large calorific value can be installed in ** with an another test head 100, and the advantage which can take arrangement of installing only a test head 100 in a clean room is acquired. Moreover, since a signal is delivered and received with a lightwave signal, it is not necessary to prepare a terminator in a signal-transmission way. Therefore, the advantage which can constitute a testing device with little calorific value is also acquired.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The connection situation of a test head 100 and a mainframe 200 is shown in drawing 9 . It connects by the cable group 300 between a main frame 200 and a test head 100. Since various kinds of signal lines exist between a mainframe 200 and a test head 100 as drawing 7 explained, the number of the cable contained by the cable group 300 increases.
[0011] Moreover, it is in the inclination which the number of terminals of a device increases with improvement in the degree of integration of a semiconductor integrated circuit device. Furthermore, improvement in a working speed and the number of the cable of the cable group 300 which connects between a main frame 200 and test heads 100 for a certain reason are in the inclination of an increment. for example, in a testing device with the test capacity for 1000 terminals The number of the signals delivered and received between a mainframe 200 and a test head 100 attains to tens of thousands of numbers. Rapidity, high degree of accuracy, noise-proof nature, etc. are taken into consideration to each. And a twisted pair, since special cables, such as a coaxial cable and multiplex shielding, are used -- a substantial conductor -- a number will be several times the number of signals, and the cable group 300 serves as a huge bundle, and makes difficult migration of a test head 100, such as etc., anchoring of a handler -- demounting.
[0012] Moreover, if the cable group 300 is lengthened, the cross talk between cables will also increase, and there is also un-arranging [which degrades trial precision]. Furthermore, since large power is needed for transmitting these signals of a lot of, this means the increment in calorific value, and makes cooling difficult and the number of terminator machines also increases, it is the factor which checks the miniaturization of a system.
[0013] The purpose of this invention tends to offer the integrated-circuit device testing device which can also suppress generating of the cross talk between signals while it minimum-izes the cable group which connects between a main frame and test heads and makes the handling of a test head easy.

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MEANS

[Means for Solving the Problem] All or some of signal-transmission way between a mainframe and a test head is transposed to the lightwave signal transmission line suitable for high-speed transmission, and it constitutes from this invention so that the signal between a mainframe and a test head may be made to deliver and receive with a lightwave signal. The data or the various timing signals which are sent into a test head from a main frame in this invention and which are set up for every terminal are transmitted by the serial signal of light, the serial receiving means formed in the test head side receives, and while changing into a parallel signal and storing in a setting register, measurement data and the integrated-circuit device testing device which considered the measurement result as the configuration returned with a lightwave signal are offered.
[0015] Pattern memory and a waveform shaping circuit are further established in a test head side, the digital test pattern data which a pattern generator outputs are transmitted to a test head by the serial signal of light, and pattern memory is made to memorize in this invention. With test initiation, the test pattern data memorized in this pattern memory are read, it changes into the pattern signal of an analog in that test pattern data (digital signal) and waveform shaping circuit that were read, and the integrated-circuit device testing device constituted so that this pattern signal might be impressed to the examined device DUT through a driver group is offered.
[0016] since that diameter is 200 - 500micrometer phi extent and does not need a go and return conductor for every channel like an electrical signal, even if a lightwave signal transmission line uses a plastic optical fiber according to the configuration of this invention -- the gestalt of a signal-transmission way -- minor-diameter-izing -- and it can lightweight-ize. Since the number of an optical fiber can be lessened by considering as the configuration delivered and received especially by the serial signal of light, the path of a cable group can be further made small and lightweight-ization can also be attained. Moreover, an optical fiber does not have generating of a cross talk mutually, in order that light may transmit only a part for a core. Therefore, the advantage which can lengthen extended distance is also acquired.
[0017]
[Embodiment of the Invention] One example of this invention is shown in drawing 1 . Drawing shows the configuration of the part (this part is called the pin unit PUN below) which carries out the analog comparison of the signal which supplied the pattern signal to one terminal by the side of a test head 100 (one terminal P of the examined device DUT), and was outputted from this terminal, and is sent to a mainframe 200.
[0018] In addition to the relay matrix 105, in this example, the cases where the local pin controller 111, the direct-current trial unit 112, and the optical input/output module 113 are formed are indicated to be driver 103A which drives one terminal P of the examined integrated-circuit device DUT and analog comparator 104A, and pin electronics 102A which carried the load test circuit 110 to the pin unit PUN.
[0019] The optical input/output module 113 has photoelectric transducers OE1-OE5, and the electrical and electric equipment and phototransducers EO1-EO5, changes into an electrical signal the lightwave signal sent from a mainframe 200 by light and the electrical-potential-difference converters OE1-OE5,

and performs a functional test and a direct-current trial using the electrical signal. Serial signal transceiver circuit 111A which receives the serial signal with which the local pin controller 111 is sent through light and the electrical-potential-difference converter OE1 from an optical fiber OPF1, With the register groups 111B, 111C, and 111D which incorporate various kinds of setting data received by this serial signal transceiver circuit 111A, and the setting data incorporated to register group 111B For example, DA converter 111E which generates the comparison electrical potential differences VOH and VOL given to the electrical potential differences VIH and VIL and analog comparator 104A which are given to driver 103A, Relay control circuit 111F which control the condition of the relay matrix 105 by the relay control signal incorporated to register group 111D can be provided and constituted.

[0020] That is, each electrical-potential-difference value of the comparison electrical potential differences VOH and VOL given to the electrical potential difference VIH of H logic, the electrical potential difference VIL of L logic, and analog comparator 104A which are given to driver 103A is stored in register group 111B, and it is given to DA converter 111E, and each of that electrical-potential-difference value changes into the electrical-potential-difference value of each analog by DA converter 111E, and is given to driver 103A and analog comparator 104A. Moreover, the data with which the test condition which operates the load test circuit 110 was also incorporated by register group 111B, and was incorporated by register group 111B also at the time of a load test are used.

[0021] While controlling the start of a setup of a control signal required for a direct-current trial, for example, the mode (voltage-source-current-measurement mode / current-source-voltage-measurement mode) applied-voltage current value of a direct-current trial, a setup of a measurement range, a setup of a clamp value, and measurement, a stop, etc. to register group 111C at the time of a direct-current trial, the test result of a direct-current trial is stored. This test result is changed into a lightwave signal TX with the electric-phototransducer E01 through serial signal transceiver circuit 111A if needed, and is transmitted to a mainframe 200.

[0022] The control signal which controls the relay matrix 105 is stored in register group 111D, this control signal is inputted into relay control circuit 111F, the relay matrix 105 is controlled, and it controls in the change condition corresponding to test mode. That is, driver 103A and analog comparator 104A are connected to the terminal P of the examined integrated-circuit device DUT at the time of a performance test, and it separates the direct-current trial unit 112. Moreover, control which detaches pin electronics 102A and instead connects the direct-current trial unit 112 to Terminal P is performed at the time of a direct-current trial.

[0023] Thus, the local pin controller 111 sets the conditions which should be set to each terminal P of every according to test mode as the register groups 111B, 111C, and 111D. Since the data incorporated by the register groups 111B, 111C, and 111D are sent by the serial signal RX of light, one optical fiber OPF1 is sufficient as that transmission line, and the lightwave signal RX sent through this optical fiber OPF1 is changed into an electrical signal by the photoelectric transducer OE1, and is inputted into serial signal transceiver circuit 111A. In addition, in this example, each setting data incorporated by the register groups 111B, 111C, and 111D is read if needed, and is changed into a lightwave signal TX with the electric - phototransducer EOI, that lightwave signal TX is returned to a mainframe through an optical fiber OPF2, and the case where it constitutes so that it can collate whether it was correctly set up by the mainframe side is shown.

[0024] An optical fiber OPF3 constitutes a pattern signal-transmission way, and the pattern signal given to Terminal P through this pattern signal-transmission way is sent with a lightwave signal PAT. This pattern signal PAT is changed into an electrical signal by the photoelectric transducer OE2, it gives driver 103A carried in pin electronics 102A, and Terminal P is given from driver 103A.

[0025] The driver control signal DRE which controls the condition of driver 103A at the time of functional test activation is sent to an optical fiber OPE4. When taking out responded output from the examined integrated-circuit device DUT with this driver control signal DRE, the output terminal of driver 103A is controlled in the condition of a high impedance, and it enables it to incorporate a responded-output signal to analog comparator 104A effectively.

[0026] The strobe pulse which compares each level of H logic and L logic in analog comparator 104A is

sent to optical fibers OPE5 and OPE6 by lightwave signal STRB-H and STRB-L. A pulse for lightwave signal STRB-H to carry out the strobe of the period of H logic of the signal read from the examined device DUT and lightwave signal STRB-L are the pulses for carrying out the strobe of the period of L logic.

[0027] These optical fiber STRB-L and STRB-H are changed into an electrical signal by photoelectric transducers OE5 and OE6, and are given to an analog comparator 110 as a strobe pulse. Optical fibers OPF7 and OPF8 constitute the transmission line for returning a strobe pulse to a main frame 200 from a test head 100. The time delay to which R-STRB-H and R-STRB-L go back and forth between analog comparator 104A from a mainframe 200 is given by the circuit where this strobe pulse returned is actual, and is used as a strobe pulse of the logic comparator prepared in a mainframe 200. That is, in order to make the time delay and time delay of a strobe pulse agree, the strobe pulse is made to go back and forth between a main frame and test heads, although the judgment result of analog comparator 104A is changed into a lightwave signal through optical fibers OPF7 and OPF8, it is sent to a main frame and it is inputted into a logic comparator. The test result of the functional test of the integrated-circuit device DUT is returned to a mainframe 200 as SH and SL at optical fibers OPF9 and OPF10, the judgment result, i.e., this example, of analog comparator 104A.

[0028] According to the example shown in drawing 1 , transfer of the signal between a mainframe 200 and a test head 100 is realizable for every [of the examined integrated-circuit device DUT] 1 terminal P with ten optical fibers so that clearly from the above explanation. A diameter is comparatively thick, for example, even if it uses the plastic optical fiber of 500micrometer phi, even if it bundles ten optical fibers, it cannot but be few diameters, and becomes a cable bundle with the bundle of 10,000 optical fibers sufficiently thinner than the cable group 300 (refer to drawing 9) of an electrical cable also as a part for 1000 terminals.

[0029] Drawing 2 shows the structure of the pin unit PUN in the case of carrying out unitization of the element of each part shown in drawing 1 for every terminal. The connector 115 grade which performs connection isolation with the integrated circuit device which constitutes the local pin controller 111 explained by drawing 1 , the integrated circuit device 112 which constitutes a direct-current trial unit, driver 103A, analog comparator 104A and pin electronics 102A that contained the load test circuit 110, the relay matrix 105, the optical input/output module 113, the electrical connector 114 that receives supply of a power source, and a PAFOMANSU board is contained to the wiring substrate within a case, and it is constituted. 116 shows a heat dissipation block.

[0030] An example of structure which mounts the pin unit PUN in a test head 100 at drawing 3 is shown. 121 shown in drawing 3 shows optical-electrical-and-electric-equipment compound substrate. This optical-electrical-and-electric-equipment compound substrate 121 has the optical fiber buried layer 123 in one field of the multilayered electric wiring plate 122, as shown in drawing 4 . The edge of the optical fiber OPF embedded at this optical fiber buried layer 123 is cut at 45 degrees. It constitutes so that the light which arranges the cutting plane S1 to the sense of the electric wiring plate 122, and transmits an optical fiber OPF may be reflected in the direction which intersects perpendicularly with the plate surface of a patchboard. The optical input/output module 113 with which the pin unit PUN was equipped is arranged in the reflective direction, and an optical fiber OPF and the optical input/output module 113 of the pin unit PUN are optically combined with it.

[0031] The other end of an optical fiber OPF can connect between a main frame 200 and the pin units PUN prepared in a test head 100 side by the optical transmission line by making it expose to the end face of a patchboard, and combining optically the fiber optic cable 124 (referring to drawing 3) extended by this exposure S2 from the main frame 200 (not shown to especially drawing 3 R> 3). In addition, about the electrical connector 114 prepared in the pin unit PUN, according to the usual electrical connection structure, it connects with the electric wiring plate 122 electrically, and connects with a mainframe 200 through the electric wiring plate 122.

[0032] The electrical cable for current supply with which 125 shown in drawing 3 was extended from the main frame 200, the optical coupling section which prepared 126 in the plate surface of optical-electrical-and-electric-equipment compound substrate 121, and 127 show an electrical connector. The

optical input/output module 113 and electrical connector 114 which formed the pin unit PUN in these optical coupling section 126 and an electrical connector 127 are connected, and the pin unit PUN is connected to a mainframe 200.

[0033] To the plate surface of optical-electrical-and-electric-equipment compound substrate 121, many optical coupling sections 126 and electrical connectors 127 are arranged, and it constitutes so that a desired number of pin units PUN can be mounted. In addition, although the example which used optical-electrical-and-electric-equipment compound substrate 121 for connection between the pin unit PUN and a fiber optic cable 124 in **** was explained, even if it does not necessarily use optical - electrical-and-electric-equipment compound substrate 121, it is good also as structure of mounting an optical connecter in the plate surface of an electric wiring plate, and making connection between the pin unit PUN and a fiber optic cable 124. Moreover, without using a patchboard, an optical connecter and an electrical connector can be connected to the edge of a fiber optic cable 124 and an electrical cable 125, and a fiber optic cable 124 and an electrical cable 125 can also be made into the structure linked to the direct pin unit PUN.

[0034] 128 shown in drawing 3 shows a cooling frame with the function which cools the pin unit PUN while supporting the pin unit PUN mechanically. This cooling frame 128 has much unit receipt hole 128A. The wall surrounding the peripheral surface of unit receipt hole 128A is made into dual structure, and it constitutes the interior so that cooling water can circulate. 128B and 128C show the feed hopper and exhaust port of cooling water.

[0035] An electrical connector 115 is formed in the upper limit side of the pin unit PUN, and the pin unit PUN is electrically connected to a performance board 101 by this electrical connector 115. In addition, in the example of drawing 3 , when two or more sets of pin unit PUN-A are directly carried in the top face of a performance board 101 and it examines especially a high-speed component, the case where it constitutes so that the electric wiring between pin units may be connected with the examined integrated-circuit device DUT in the state of the shortest and a trial may be possible is shown by operating this pin unit PUN-A.

[0036] Drawing 5 shows other examples of a test head 100. Using the lightwave signal transmission line being excellent in rapidity, a pattern data signal is also transmitted by the serial signal, and it returns to a parallel signal by the test head 100 side, and it constitutes from this example so that a pattern data signal may be generated. That is, in this example, about the local pin controller 111 and the direct-current trial unit 112, although it is the same as the example of drawing 1 , it considers as the structure which transferred the function of some waveform shaping circuits, logical-comparison circuits, and timing generators to the test head 100 side from the mainframe side about the test pattern signal system.

[0037] That is, the wave controller 130 is formed out of the local pin controller 111 and the direct-current trial unit 112, and it constitutes so that this wave controller 130 may be made to perform generating and logical-comparison actuation of a pattern signal. For this reason, the serial signal transceiver circuit 131 is established also in the wave controller 130, the serial signal of the pattern data PATDAT sent by this serial signal transceiver circuit 131 from a pattern generator 201 is received from an optical fiber OPF6, it changes into a parallel signal, a waveform shaping circuit 132 is given, and the pattern signal which has an analog wave in a waveform shaping circuit 132 is made to generate.

[0038] A timing generator 133 shows the case where only the configuration of the fine delay circuit DY2 explained by drawing 7 is transferred to a test head side. That is, by relocating only the fine delay circuit DY2 to a test head 100 side, it is small in the circuit scale of the timing generator transferred to a test head 100, and considers as the structure which avoided large-sized-ization of a test head 100. Therefore, in this example, the rate pulse RAT to which the coarse delay which makes the period of Clock CLK a unit by the coarse-delay circuit DY1 was given by the mainframe 200 side shall be outputted with a lightwave signal, and this rate pulse RAT shall be sent through an optical fiber OPF4. This lightwave signal is changed into the rate pulse RATE by the photoelectric transducer OE3, and this electric rate pulse RATE is given to a timing generator 133, and with this timing generator 133, fine delay is given and it is distributed as a timing signal of each part. Fine lag data TMFIN is inputted into the timing controller 135 through the serial signal transceiver circuit 131 from an optical fiber OPF5,

and a timing generator 133 is controlled by the timing controller 135.
[0039] In the logical-comparison circuit 134, logical comparison of the pattern data PATDAT (digital signal) inputted into a waveform shaping circuit 132 and the reply signal which an examined integrated-circuit device outputs is carried out, the comparison result is given by the electric-phototransducer OE5 from delivery and the serial signal transceiver circuit 131 as a fail signal FDAT in the serial signal transceiver circuit 131, and it changes into a lightwave signal, and is sent out to an optical fiber OPF7.
[0040] Drawing 6 shows the example of further others of this invention. In this example, along with the wave controller 130, the timing memory TM, the pattern memory PM, and the fail memory FM are formed, and the case where it constitutes so that a pattern signal may be generated by the test head 100 side is shown. That is, the pattern memory PM is made to send in and memorize beforehand the pattern data given to one terminal P of the examined integrated-circuit device DUT to a test head 100 through an optical fiber OPF5 by the serial signal. Furthermore, the timing memory TM is made to also send in and memorize timing data through an optical fiber OPF5 using a part of time amount of the serial signal RXX with the pattern data. Therefore, each pin unit PUN prepared in the test head 100 is made to send in and memorize the data for all terminals from a mainframe 200 side before test initiation.
[0041] Pattern data are read from the pattern memory PM with test initiation, and the pattern data is changed into the pattern signal which has an analog wave in a waveform shaping circuit 132. Moreover, it is read to coincidence, and rate signal RATE which expresses a test period with a timing generator 133 is delayed, various kinds of timing signals are generated, the timing signal is distributed to a waveform shaping circuit 132, analog comparator 104A, and logic-comparator 134 grade, and the timing memory TM specifies the timing of each comparison actuation, the standup of a pattern signal, the timing of falling, etc.
[0042] Whenever an inequality occurs in a logic comparator 134, the signal of for example, H logic which expresses a defect with the defect generating address of the fail memory FM is written in. The fail data (test result) incorporated by the fail memory FM use the idle time under trial, or are changed into a lightwave signal TXX with the electric - phototransducer EO2 through a memory bus MBUS and the serial signal transceiver circuit 131 at the time of test termination, and are sent to a mainframe 200 through an optical fiber OPF6.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram for explaining one example of this invention.
[Drawing 2] The perspective view for explaining an example of the structure of the pin unit used in the example shown in drawing 1 .
[Drawing 3] The perspective view for explaining an example of structure which mounts the pin unit shown in drawing 2 .
[Drawing 4] The sectional view for explaining an example of optical-electrical-and-electric-equipment compound substrate shown in drawing 3 .
[Drawing 5] The block diagram for explaining other examples of this invention.
[Drawing 6] The block diagram for explaining the example of further others of this invention.
[Drawing 7] The block diagram for explaining a Prior art.
[Drawing 8] The wave form chart for explaining actuation of a Prior art.
[Drawing 9] The perspective view for explaining a Prior art.
[Description of Notations]
100 Test Head
PUN Pin unit
111 Local Pin Controller
111A, 131 Serial signal transceiver circuit
111B-111D Register group
111F Relay control circuit
112 Direct-Current Trial Unit Prepared in Test Head
113 Optical Input/output Module
130 Wave Controller
132 Waveform Shaping Circuit
133 Timing Generator
134 Logical-Comparison Circuit
135 Timing Troller
136 Memory Bus Controller

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 2]

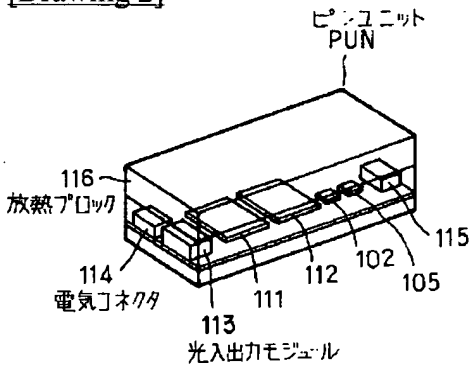


図 2

[Drawing 8]

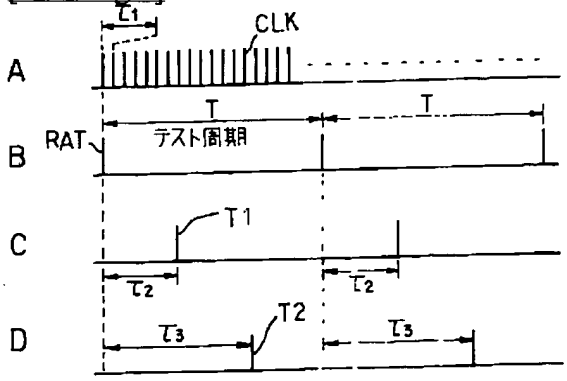
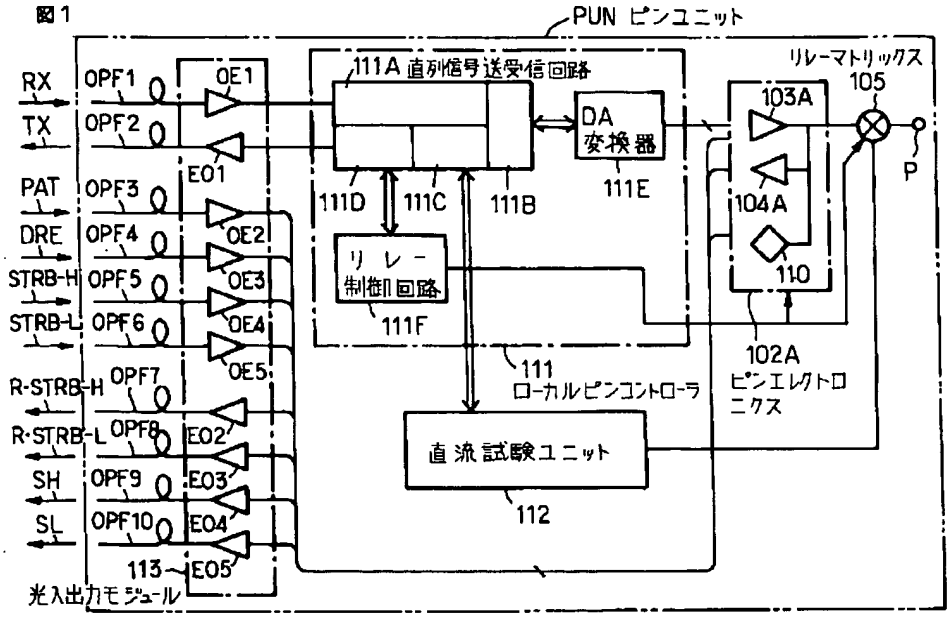


図 8

[Drawing 1]



[Drawing 3]

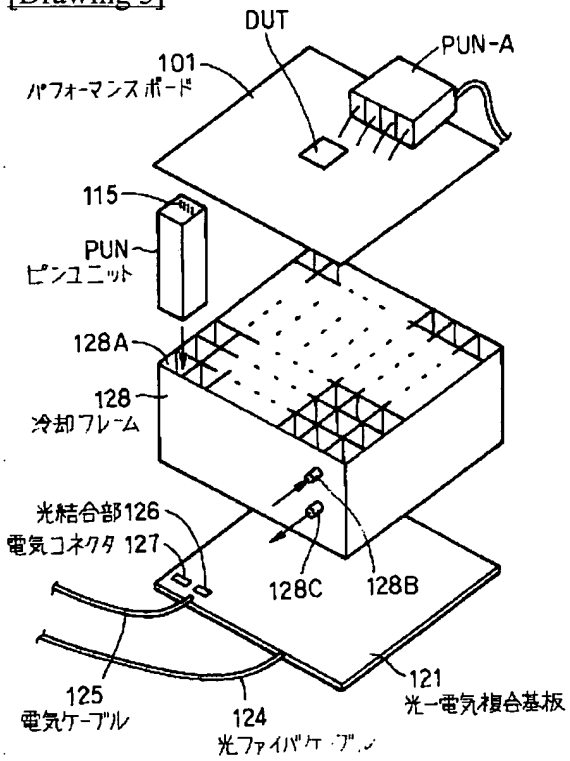
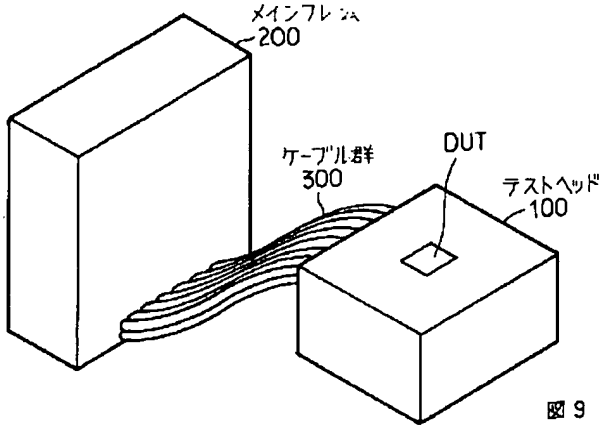


図3

[Drawing 9]



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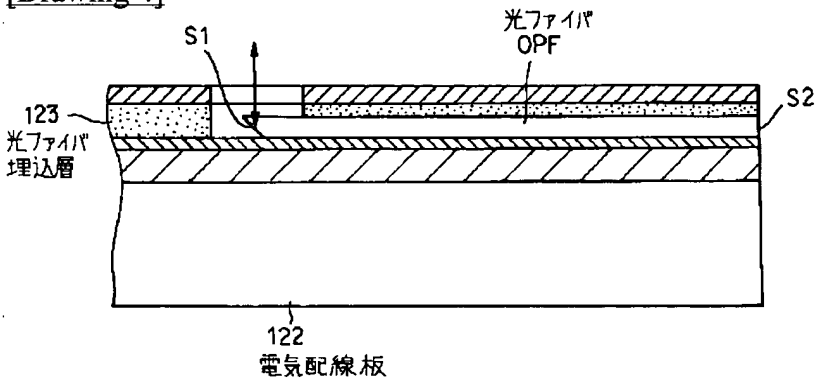
[Drawing 4]



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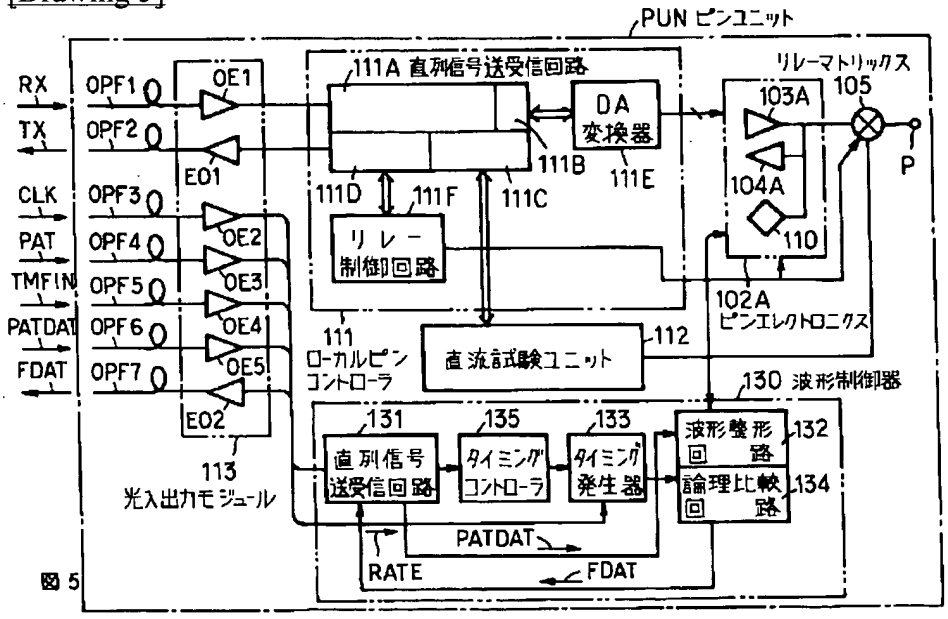
[Drawing 5]



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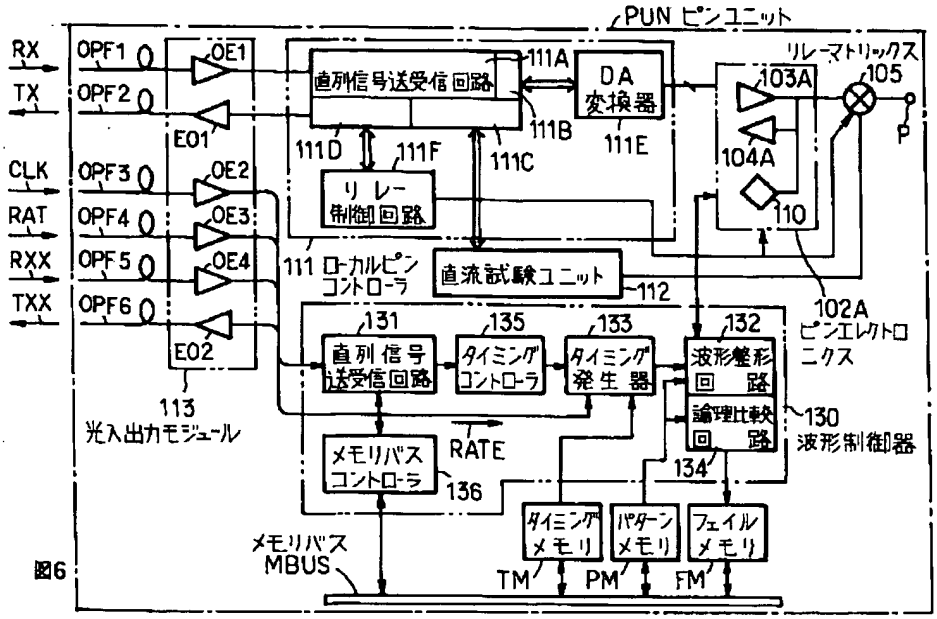
[Drawing 6]



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[Drawing 7]

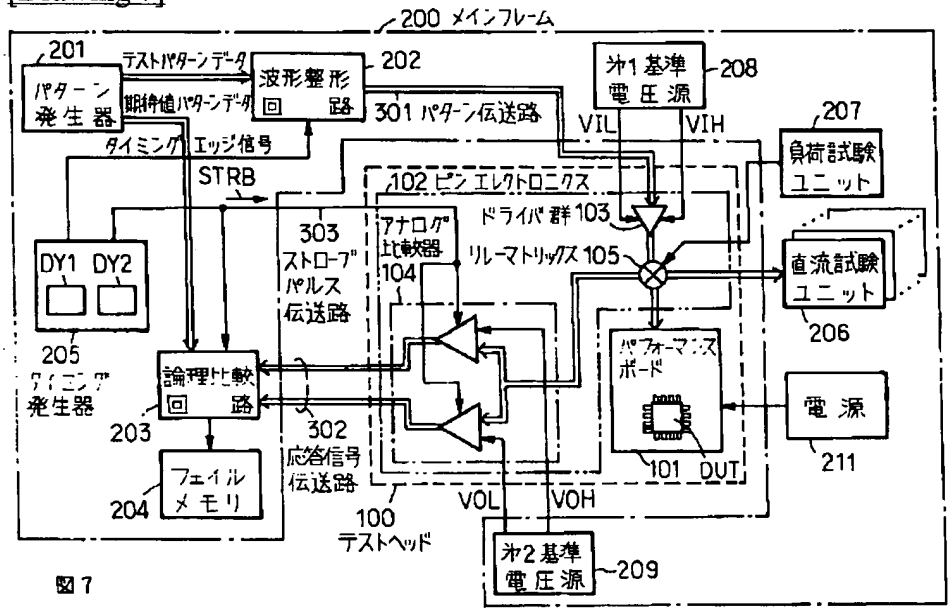

図7

[Translation done.]